JXR231MT User Manual

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1 General Description

The JXR231MT is an extremely accurate, IIC real-time clock (RTC) chip with built-in 32.768kHz digital temperature compensated crystal oscillator (D-TCXO). The minimum time unit is millisecond, and the automatic leap year correction is available. The JXR231MT can also provide a timed alarm interruption, fixed-cycle interruption, time update interrupt output and frequency output at 32.768kHz, 1024Hz, 32Hz and 1Hz.

The chip operating temperature range covers -45℃ ~ 125℃ and provides ultra-high precision clock output over temperature range of -45℃ ~ 105℃, and can provide absolute accuracy of ±1℃ of temperature output. With the function of automatic switching function of backup power supply, it automatically switches the backup power supply to supply power for the chip after the main power domain is powered done.

2 Features

- Built in extremely accurate 32.768kHz D-TCXO
- ms-level timing accuracy
- Fast (400kHz) IIC Interface
- Operating Temperature Range of -45℃ ~ 125℃
- High frequency stability:
  - 25℃ : < 1.0ppm; (daily timing error is less than 0.086s)
  - 0℃ ~ 50℃ : < 3.0ppm; (daily timing error is less than 0.259s)
  - -45℃ ~ 85℃ : < 5.0ppm; (daily timing error is less than 0.432s)
  - 85℃ ~ 105℃ : < 8.0ppm; (daily timing error is less than 0.691s)
- Time alarm interruption (The interval can be set to week, day, hour and minute)
- Fixed-cycle interruption
- Time update interruption
- Frequency output at 32.768kHz, 1024Hz, 32Hz and 1Hz with enable control
- Calendar range supports 2000-2099, with automatic leap year correction
- Temperature compensation circuit operating voltage range:2.2V ~ 5.5V
- Clock circuit operating voltage range:1.0V ~ 5.5V
- Built-in 64Byte user RAM
- Low current consumption: 0.9μA@3V(Typ)

3 Block Diagram

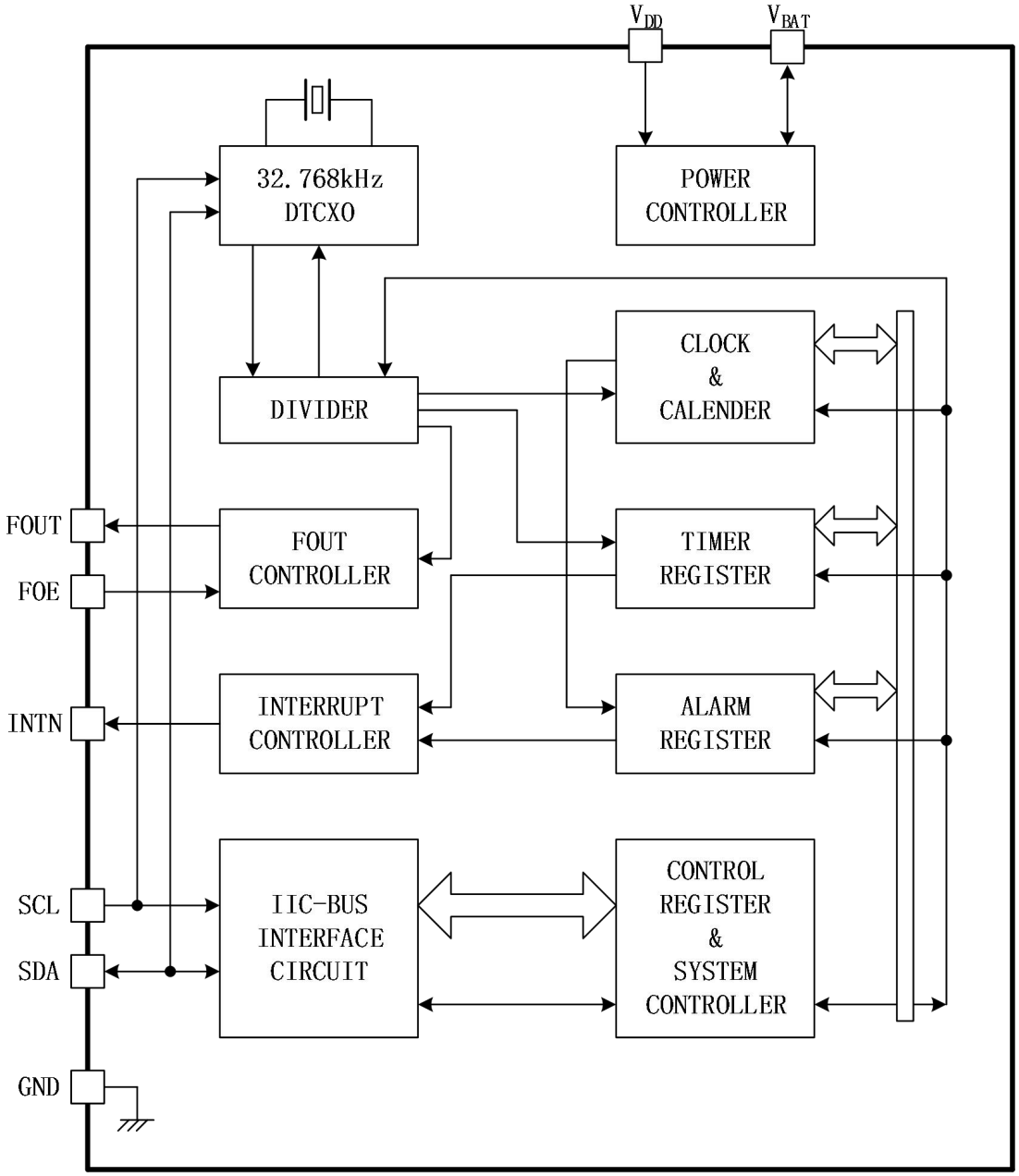


Figure 3- 1 JXR231MT Block Diagram

4 Pin Definitions

4.1 Pin Configuration

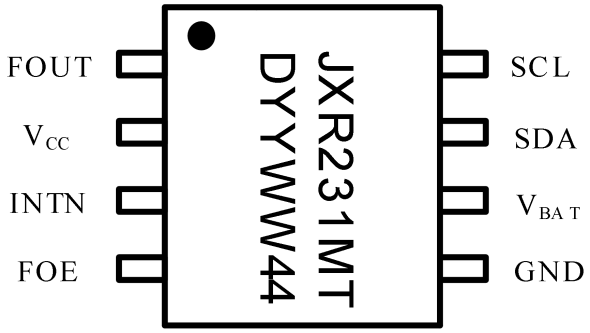


Figure 4- 1 JXR231MT Pin Configuration

4.2 Pin Description

Table 4- 1 JXR231MT Pin Description

Pin name	I/O	Function
1. FOUT	OUTPUT	32.768kHz output controlled via FOE. When FOE = '1', FOUT outputs frequency at 32.768kHz. When FOE = '0', FOUT is low.
2. V_{DD}	POWER	DC Power Pin for Primary Power Supply.
3. INTN	OUTPUT	Interrupt output port, N-ch open-drain output.
4. FOE	INPUT	FOUT output enable pin. When FOE = '1', FOUT is frequency output.
5. GND	GROUND	Ground
6. V_{BAT}	POWER	Backup Power-Supply Input. If the backup power automatic switching function is not required, this pin should be shorted to VDD.
7. SDA	INOUT	Serial-Data Input/Output. This pin is the data input/output for the IIC serial interface, N-ch open-drain output.
8. SCL	INPUT	Serial-Clock Input. This pin is the clock input for the IIC serial interface

5 Absolute Electrical Specifications

Table 5- 1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply Voltage*1	V_{DD}	Voltage between V_{DD} and GND	-0.5 to 6	V
Input Voltage*1, *2	V_{IN}	FOE, SCL, SDA pins	-0.5 to V_{DD} + 0.5	V
Output Voltage*1, *2	V_{OUT}	FOUT, SDA, INTN pins	-0.5 to V_{DD} + 0.5	V
Storage Temperature Range	T_{STG}	Dispersed, unpackaged	-55 to 125	ºC

*1：Each electrical specifications should not exceed the maximum rating range in the table above at any time, otherwise it will cause deterioration of the relevant parameters, decrease in reliability or even chip failure.

*2：V_{DD} here refers to the V_{DD} range under recommended operating conditions.

6 Recommended Operating Conditions

Table 6- 1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	Interface Voltage	1.5	3.0	5.5	V
Temperature Compensation operating Voltage	V_{TEM}	Temperature-Compensation Circuit Operating Voltage	2.2	3.0	5.5	V
Clock Operating Voltage	V_{CLK}	Oscillator Module Operating Voltage	1.0	3.0	5.5	V
Temperature Compensation Range	V_{COMP}	Temperature Compensation Range	-45	25	105	ºC
Operating Temperature	T_{OPR}	---	-45	25	125	ºC

* Any operation outside of the recommended ranges in the table above may significantly affect the reliability of the chip.

7 Frequency Characteristic

Table 7- 1 Frequency Characteristics

Item	symbol	Condition	MIN	MAX	Unit
Frequency Stability	Δf/f	Ta = 25 ºC, V_{DD} = 3.0V	-1.0	+1.0	$\times10^{-6}$
		Ta = 0 ºC ~ 50 ºC, V_{DD} = 3.0V	-3.0	+3.0	
		Ta = -45 ºC ~ 85 ºC, V_{DD} = 3.0V	-5.0	+5.0	
		Ta = 85 ºC ~ 105 ºC, V_{DD} = 3.0V	-8.0	+8.0	
		Ta = 105 ºC ~ 125 ºC, V_{DD} = 3.0V	-80.0	+10.0	
Voltage Coefficient	Δf/f/V	Ta = 25 ºC, V_{DD} = 2.2V ~ 5.5V	-1.0	+1.0	$\times10^{-6}$/V
Starting Time	T_{STA}	Ta = 25 ºC, V_{DD} = 1.5V ~ 5.5V		1.0	s
		Ta = -40 ºC ~ 85 ºC, V_{DD} = 1.5V ~ 5.5V		2.0	
Aging	fa	Ta = 25 ºC, V_{DD} = 3.0V, first year	-1.0	+1.0	$\times10^{-6}$/year

8 Electrical Characteristics

8.1 DC Electrical Characteristics

Table 8- 1 DC Electrical Characteristics

* Typical values are at GND = 0V, V_{DD} = 1.5V ~ 5.5V, Ta = -40 ºC ~ 85 ºC, unless otherwise noted.

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current Consumption	I_{DD1}	FOE = GND FOUT = '0'	V_{DD} = 5V		1.2	3.0	μA
	I_{DD2}		V_{DD} = 3V		0.9	2.0	
Current Consumption	I_{DD3}	FOE = V_{DD} FOUT = 32.768kHz CL = 0pF	V_{DD} = 5V		3.6		μA
	I_{DD4}		V_{DD} = 3V		2.9		
Current Consumption	I_{DD5}	FOE = V_{DD} FOUT = 32.768kHz CL = 30pF	V_{DD} = 5V		7.5		μA
	I_{DD6}		V_{DD} = 3V		6.2		
Current Consumption	I_{DD7}	During IIC communications, V_{DD} = 5V				5.0	μA
High Input Level Voltage	V_{IH}	FOE, SCL, SDA pins	V_{DD} = 2.2V ~ 5.5V	0.7*V_{DD}		V_{DD}+0.3	V
Low Input Level Voltage	V_{IL}	FOE, SCL, SDA pins	V_{DD} = 2.2V ~ 5.5V	-0.3		0.3*V_{DD}	V
High Output Level Voltage	V_{OH}	FOUT pin	I_{OH} = -1mA	V_{DD}-0.3		V_{DD}	V
Low output Level Voltage	V_{OL}	FOUT, INTN pins	I_{OL} = 1mA	GND		GND+0.3	V
		SDA pin	$V_{DD} \geq$ 2V I_{OL} = 3mA	GND		GND+0.3	V
Input Leakage Current	I_{LK}	FOE, SCL, SDA, V_{IN}=V_{DD} or GND		-0.1		0.1	μA
Output Leakage current	I_{OZ}	INTN, FOUT, SDA, V_{IN}=V_{DD} or GND		-0.1		0.1	μA

8.2 AC Electrical Characteristics

Table 8- 2 AC Electrical Characteristics

* Typical values are at GND = 0V, V_{DD} = 1.5V ~ 5.5V, Ta = -40 °C ~ 85 °C, unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	---			400	kHz
Starting Condition Setup Time	$t_{SU;STA}$	---	0.6			μs
Starting Condition Hold Time	$t_{HD;STA}$	---	0.6			μs
Data Transfer Setup Time	$t_{SU;DAT}$	---	100			ns
Data Transfer Hold Time	$t_{HD;DAT}$	---	0		700	ns
Termination Condition Setup Time	$t_{SU;STO}$	---	0.6			μs
Bus Free Time	t_{BUF}	Between STOP and START Conditions	1.3			μs
Low Period of SCL	t_{LOW}	---	1			μs
High Period of SCL	t_{HIGH}	---	1			μs
SCL and SDA Rise Time	t_r	---			0.3	μs
SCL and SDA Fall Time	t_f	---			0.3	μs
Spike Time on Bus	t_{SP}	---			50	ns
FOUT Output Duty Cycle	Duty	Calculated with output up to 50% of V_{DD}	40	50	60	%

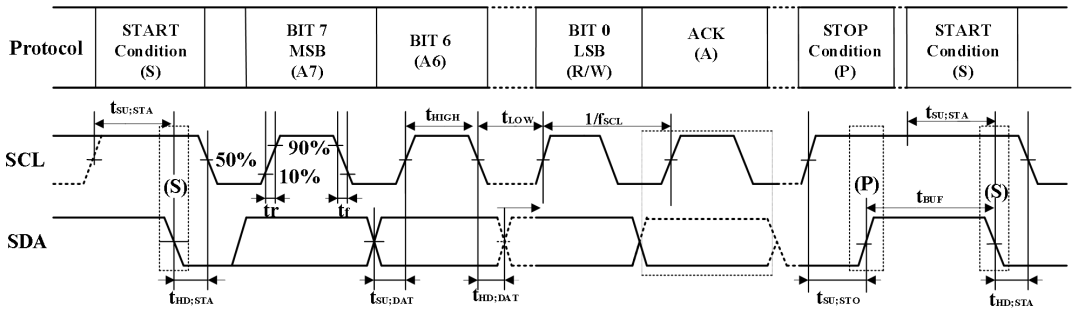


Figure 8- 1 IIC Timing

*The IIC data transfer is located between the STOP and START Conditions, the data transfer operation must be completed within 0.95s, after exceeding this event, the IIC bus will have an internal timer reset.

9 Registers

9.1 Registers Overview

Table 9- 1 Registers Summary Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70	MSEC[9:8]	○	○	○	○	○	○	512	256
71	MSEC[7:0]	128	64	32	16	8	4	2	1
00 or 10	SEC	○	40	20	10	8	4	2	1
01 or 11	MIN	○	40	20	10	8	4	2	1
02 or 12	HOUR	○	○	20	10	8	4	2	1
03 or 13	WEEK	○	6	5	4	3	2	1	0
04 or 14	DAY	○	○	20	10	8	4	2	1
05 or 15	MONTH	○	○	○	10	8	4	2	1
06 or 16	YEAR	80	40	20	10	8	4	2	1
07	RAM	●	●	●	●	●	●	●	●
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	●	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0B or 1B	TimerCounter0	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	○	○	XST
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET
17	Temp Int	SIGN	64	32	16	8	4	2	1
18	Temp Frac	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
19	PW Control	CHGEN	INIEN	○	○	○	SWSEL	SMPT1	SMPT0
1A	Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0

*Make sure to write legal values to the calendar and clock registers, otherwise the chip will not be able to perform correct timing operations.

*The register bits labeled '○' is a read-only bit with a read value of '0'. Writing '1' to the read-only bit is prohibited. The register bits labeled '●' can be used as RAM to perform read and write operations.

*If the alarm interrupt function is not set (AIE = '0'), register 8~A can be used as RAM.

*If the interval timer interrupt function is not set (TE = TIE = '0'), register 0B or 1B and 0C or 1C can be used as RAM.

*UF, TF, AF and XST bits are only allowed to be written to '0'.

*When the chip is powered up, the CSEL0 bit is preset to '1', the FSEL1, FSEL0, CSEL1, UIE, TIE and AIE are preset to '0'.

* MSEC[9:8] and MSEC[7:0] are read-only registers.

9.2 Register Details

9.2.1 Clock and Calendar Registers (00 ~ 06 or 10 ~ 16)

- Data Structure

The contents except the week register are in the binary-coded decimal (BCD) format. For example, the value “0101 1001” of the Second register represents the current time is 59 second.

The timing system is fixed to 24-hour system.

- Year registers and leap years

The time range of the year register is 00 - 99. After 99, it overflows back to 00. When the value represented by the year register is divisible by 4, the year is recognized as a leap year. The valid time range of the calendar is 2000~2099.

- Week registers

The Day of the Week register has a total of 7 valid values, and each 1 valid bit represents one of the days from Monday to Sunday, so only one bit of this register is allowed to be '1'.

Table 9- 2 Week Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Week
0	0	0	0	0	0	1	Sun.
0	0	0	0	0	1	0	Mon.
0	0	0	0	1	0	0	Tues.
0	0	0	1	0	0	0	Wed.
0	0	1	0	0	0	0	Thur.
0	1	0	0	0	0	0	Fri.
1	0	0	0	0	0	0	Sat.

9.2.2 Milliseconds Register (70 ~ 71)

These two registers are read-only registers and unable to write, and are used to provide ms timing for customers to get a more accurate clock than seconds. These two registers have a total of 10 valid bits (The high 2 bits are in register 70 and low 8 bits are in register 71), and the timing accuracy is (1/1024)s.

After the user configures the Seconds register, registers 70 and 71 are automatically cleared '0' and start from 0ms again.

9.2.3 Alarm Registers (08 ~ 0A)

Alarms can be set to X hours and X minutes on any day of the week or X hours and X minutes on day X of each month (weekly alarm mode and daily alarm mode), and the alarm code can be set by the WADA bit in register 0D or 1D.

Each alarm register has AE (Alarm Enable) bit (bit7). When the AE bit of a certain alarm register is '0', the set value of this register needs to be compared with the corresponding timing register, and an alarm interrupt is output when the value is the same; when the AE bit is '1', the corresponding alarm register value is ignored, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is the same as the corresponding timing register value.

When the week alarm mode is selected, the days of the week can be selected at the same time,

so the WEEK ALARM function bit0~bit6 in register 0A or 1A can have several bits '1' at the same time.

The correspondences in the WEEK ALARM mode can be referred to Table9-3.

Table 9- 3 Week Alarm Mode Register A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0A	WEEK ALARM	Sat.	Fri.	Thur.	Wed.	Tues.	Mon.	Sun.

9.2.4 Fixed-Cycle Counter Control Register (0B or 1B and 0C or 1C)

These two registers are used to set the preset countdown value for the fixed-cycle interrupt. When the value in the above two registers changes from 001h to 000h, the fixed-cycle interrupt event occurs, TF is set to '1' and a low level is output on INTN (if TIE is '1'). After that, the 0B or 1B and 0C or 1C register are reset to the preset value, and the countdown process starts again.

9.2.5 Control Register and Flag Register(0D ~ 0F or 1D ~ 1F)

- WADA bit

Alarm interrupt Mode Selection Bit. When set to '1', it is Day Alarm Mode; when set to '0', it is Week Alarm Mode.

- USEL bit

Used to set the period of the time update interrupt; this bit default to '0' when the chip is powered up.

Table 9- 4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

When this bit is set to '1', the counter for fixed-cycle interruptions starts counting down, and when it is set to '0', it stops counting down.

- FSEL bit

It is used to set the output frequency of port FOUT. Refer to Table9-5 for the specific configurations. The bits are set to '00' after the chip is powered up by default.

Table 9- 5 FOUT Output Frequency Selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768kHz *Default
0	1	1024Hz
1	0	32Hz
1	1	1Hz

- TSEL bit

Used to set the count period for fixed-cycle interrupts.

Table 9- 6 Fixed-Cycle Interrupt Count Period Selection

TSEL1	TSEL0	Source clock

0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF bit

Flag bits for alarm interrupt, fixed-cycle interrupt, and time update interrupt; when the interrupt events above occur, the corresponding flag bit is set to '1'. The flag bit will be maintained as '1' until it is cleared to '0' manually, and it is prohibited to manually set the above fig bits to '1'.

- AIE, TIE, UIE bit

They are used to set the interrupt signal output on the INTN pin when an alarm interrupt, fixed-cycle interrupt, and time update interrupt event occurs. The all three bits is set to '0' by default when the chip is powered up.

The interrupt signal output on the INTN pin is the logical and of the alarm interrupt, fixed-cycle interrupt and time update interrupt. The interrupt flag is used to determine the specific interrupt situation and to determine the interrupt signal output.

- XST bit

Oscillator stop flag. This bit is set to '1' after detecting that the crystal oscillator has stopped oscillating, causing the clock circuit to fail to time properly. This flag bit will remain '1' until it is manually cleared to '0'. Setting this flag bit to '1' manually is prohibited. This flag bit is set to '1' by default when chip is powered up, prompting the user that the current timing is not accurate and need to configure the time. After setting the time, you can set XST bit to '0' through IIC-bus, the flag bit will remain '0' until the oscillator oscillator stop event occurs.

- CSEL bit

Used to set the time interval for the temperature compensation circuit to start. This bit is set to '01' (2s) when the chip powered on.

Table 9- 7 Temperature Compensation Interval Selection

CSEL1	CSEL0	Operation interval
0	0	0.5s
0	1	2s *Default
1	0	10s
1	1	30s

- EN_DET bit

Oscillator Stop Detection function control bit. Setting this position to '1' turns on the stop oscillation detection function; setting this position to '0' turns off the stop vibration detection function, which saves about 50nA of current consumption. The default state of this control bit is '1' when chip is powered up.

- RESET bit

When RESET is set to '1', the Second and Millisecond register are reset, and the clock is stopped. Temperature compensation function is also disabled.

The RESET bit which is set to '1' will be re-cleared to '0' under the following three conditions: when an IIC stop condition is detected, a restart condition, or when the IIC bus is reset after 0.95s.

9.2.6 Temperature Registers (17, 18)

Table 9- 8 Temperature Related Registers Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17	Temp Int	SIGN	64	32	16	8	4	2	1
18	Temp Frac	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Registers 17 and 18 store the integer portion and the fractional portion of the current temperature value, where the highest bit of the register 17 is a sign bit, storing the data in the form of a 16bit signed number.

Table 9- 9 Temperature Calculation Method

SIGN	Temperature Calculation Method
0	$T = reg17[6] \times 64 + \lambda + reg17[0] \times 1 + reg18[7] \times 2^{-1} + \lambda + reg18[0] \times 2^{-8}$
1	$T = reg17[6] \times 64 + \lambda + reg17[0] \times 1 + reg18[7] \times 2^{-1} + \lambda + reg18[0] \times 2^{-8} - 128$

For example,

Register 17, 18 are 0x19 and 0x80 representing the current temperature of 25.5℃.

Register 17, 18 are 0xFB and 0xC0 representing the current temperature of -4.25℃.

9.2.7 Power Management Function Related Registers （19）

Table 9- 10 Power Management Function Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	PW Control	CHGEN	INIEN				SWSEL	SMPT1	SMPT0

- CHGEN Bit

Charging function control bit, CHGEN = '1', turn on the charging function; CHGEN = '0', turn off the charging function.

- INIEN Bit

Automatic switching function of the power supply, INIEN = '1', turn on the power supply automatic switching function; INIEN = '0', turn off the power supply automatic switching function

- SWSEL Bit

Charge switch control bit. In manual control mode, it controls the switching state between the main power supply and the backup power supply. SWSEL = '1', switch is on; SWSEL = '0', switch is off.

- SMPT1, SMPT0 Bit

Controls the size of the power detection window, 300μs/600μs/2ms/256ms optional.

* Power management features are detailed in Chapter 10.

9.2.8 Output Precision Adjustment Register (1A)

The 1A register enables the function of fine-tuning the output frequency for higher timing accuracy. Refer to the following Table9-8 for the specific adjustment range and step size.

Table 9- 11 Output Frequency Accuracy Adjustment Table

OFS3	OFS2	OFS1	OFS0	Offset Value (ppm)
0	0	0	0	0.00
0	0	0	1	-0.55
0	0	1	0	-1.10
0	0	1	1	-1.65
0	1	0	0	-2.20
0	1	0	1	-2.75
0	1	1	0	-3.30
0	1	1	1	-3.85
1	0	0	0	4.40
1	0	0	1	3.85
1	0	1	0	3.30
1	0	1	1	2.75
1	1	0	0	2.20
1	1	0	1	1.65
1	1	1	0	1.10
1	1	1	1	0.55

10 Power Management Functions

JXR231MT has dual power supply function, the dual power supply can be configured to switch automatically and the main power supply can provide trickle charge for the backup power supply.

10.1 Related Registers

The power management related registers can be found in Section 9.2.7. Table10-1 below shows the specific operation of each control bit.

Table 10- 1 Power Management Control Menu

INIEN	CHGEN	SWSEL	SW1	Description
0	X	0	OFF（0）	Initial state of power-up, single power supply
		1	ON（1）	------
1	0	X	Suitable for non-rechargeable batteries as backup power	Automatically able to control the switching state according to the power detection results, refer to the power management control flow.
	1		Suitable for rechargeable batteries as backup power	

10.2 Power Detection Module

In order to satisfy the function related to dual power supply control, the chip has built-in two independent power detection units, which are respectively used to detect whether the rechargeable battery is in the full-charge state and whether the voltage of the main power supply is higher than that of the backup power supply.

Table 10- 2 Power Management Control Menu

Symbol Name	Description
VD2	Detect the size of V_{BAT} and V_{FULL}(3.7V). When V_{BAT} is larger, the output is '1'
VD3	Detect the size of V_{BAT} and V_{DD}. When V_{BAT} is larger, the output is '1'

10.3 Power-Up Defaults

The default state of the power management part is as shown in Figure 10- 1 below, V_{BAT} is directly connected to the RTC power supply terminal, and V_{DD} is connected to the RTC power supply terminal through a diode, so it is recommended to supply the power through V_{BAT} or short V_{BAT} to V_{DD} when using a signal power supply.

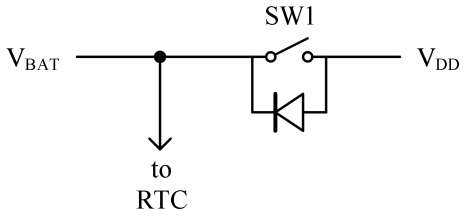


Figure 10- 1 Power-Up Defaults

10.4 Single Power Supply

As described in Section 10.3, when the chip has a single power supply, it is recommended to supply the power through V_{BAT} or short V_{BAT} to V_{DD} .

10.5 Non-Rechargeable Batteries as Backup Power

When the backup power supply is a non-rechargeable battery, it is necessary to set INIEN to '1' to turn on the power automatic switching function and set CHGEN to '0' to turn off the charging function. Table 10-3 shows the specific control method.

Table 10- 3 Control Table for Non-Rechargeable Batteries as Backup Power

Power Supply Test Results	SW1	Power Supply Status
$V_{DD} > V_{BAT}$	ON	Main power supply
$V_{DD} < V_{BAT}$	OFF	Backup power supply

10.6 Rechargeable Batteries as Backup Power

When the rechargeable battery is used as a backup power source, it is necessary to set INIEN to '1' to turn on the power automatic switching function, set CHGEN to '1' to turn on the charging function. According to the results of the two sets of power supply detection(V_{BAT} vs V_{DD}, V_{BAT} vs V_{FULL}), the power supply state is automatically switched. Where V_{FULL} is the backup power supply stop-charging voltage (about 3.7V). The control state of the switch is shown in the Table10-4 below.

Table 10- 4 Control Table for Rechargeable Batteries as Backup Power

Power Supply Test Results		SW1	State of Charge	Supply Status
$V_{DD} < V_{BAT}$		OFF	Stop charging	Backup power supply
$V_{DD} > V_{BAT}$	$V_{BAT} \geq V_{FULL}$	OFF	Stop charging	Main power supply
	$V_{BAT} < V_{FULL}$	ON	Charging	Main power supply

During power detection, it is necessary to disconnect SW1 for detection in order to ensure the accuracy of the detection results, and the size of the detection window is determined by registers SMPT1 and SMPT0.

Table 10- 5 Power Detection Window Control Table

SMPT1	SMPT0	Detection Window
0	0	300us *Default
0	1	600us
1	0	2ms
1	1	256ms

10.7 Power Management Control Flow

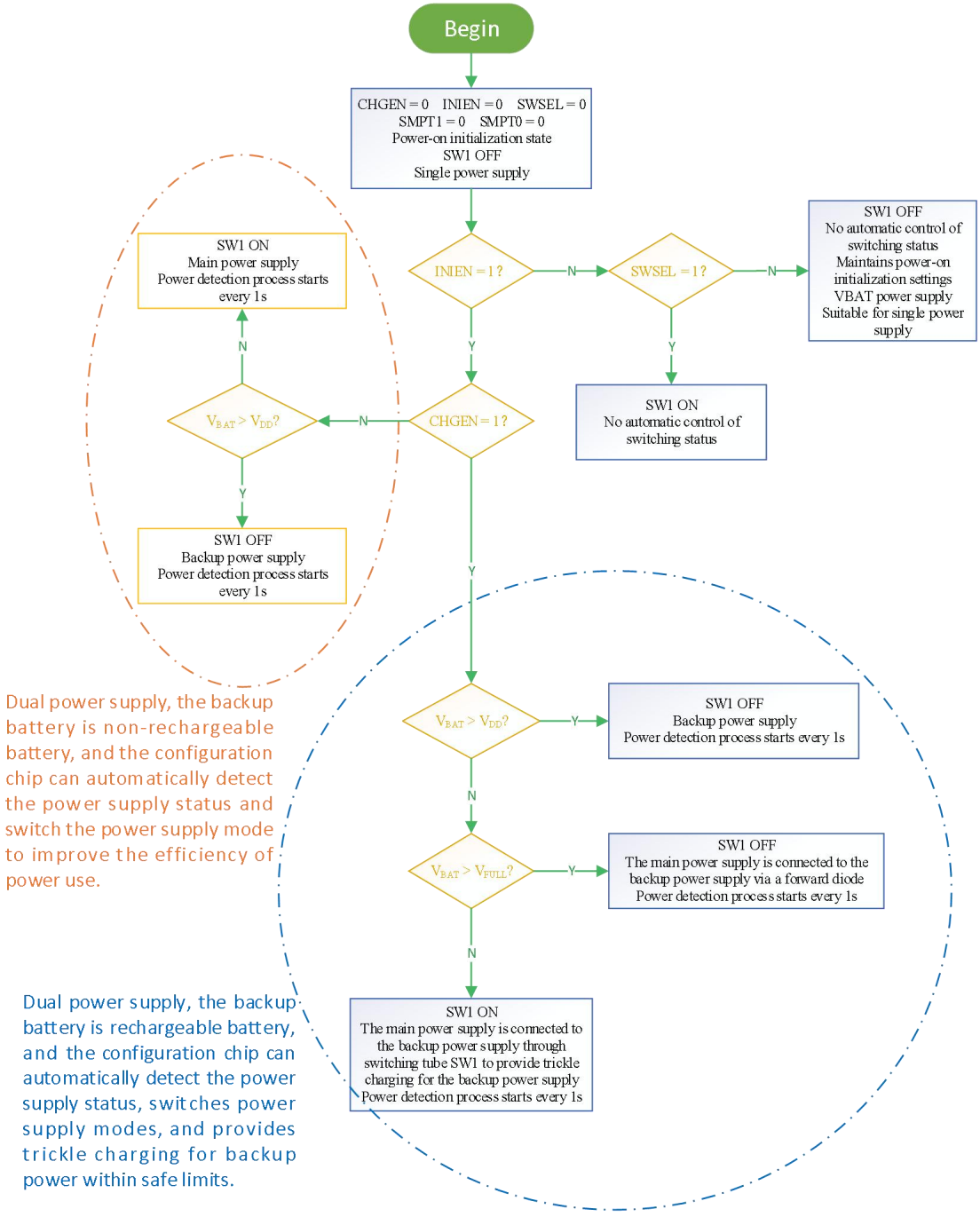


Figure 10- 2 Power Management Module Workflow Diagram

11 Interrupt Function

11.1 Alarm Interruption

Alarm interruptions can be generated on set days of the weeks, days, hours and minutes.

11.1.1 Alarm Interrupt Timing

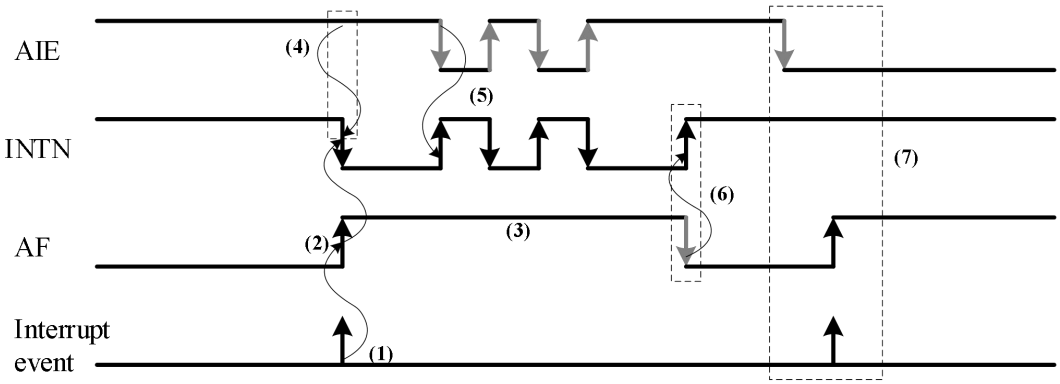


Figure 11- 1 Alarm Interrupt Timing

(1) Set the hour, minute, date or day of the week information corresponding to the alarm interruption and the WADA registers to generate an alarm interruption event when the set time matches the current time.

(2) The AF flag bit is set to '1' when an alarm interrupt event is generated.

(3) The AF register will remain at '1' until it is manually cleared to '0'.

(4) When an alarm interrupt event occurs, if AIE='1', INTN outputs a low level; if AIE='0', INTN remains in a high resistance state.

(5) If AIE is set to '0' during the INTN = '0' period, INTN will immediately return to the high resistance state; AIE can be used to control the output state of INTN before an alarm interrupt event occurs and the AF register is cleared to '0'.

(6) Setting AF register to '0' clears the alarm interrupt output and INTN instantly changes from '0' to a high resistance state.

(7) If AIE = '0' when the alarm interrupt time occurs, INTN stays high and does not output a low level.

11.1.2 Alarm Interrupt Related Registers

Table 11- 1 Alarm Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	●	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0D or 1D	Extension	○	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	**AF**	○	○	XTS
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	**AIE**	○	EN_DET	RESET

- When configuring the Alarm Interrupt Register, it is recommended to first set AIE to '0' to prevent unnecessary hardware interrupts from being generated during operation.
- WADA is used to select the alarm mode, when set to '1', it is the day alarm mode, when set to '0', it is the week alarm mode.
- The occurrence of an alarm interrupt event will set the AF flag position '1', which will remain at '1' until it is manually set to '0'.
- When an alarm interrupt event occurs, the AIE decides whether or not to generate an interrupt signal output (When AIE = '1', INRN = '0'; When AIE = '0', INTN = Hi-Z).
- AE bit of '0' indicates that the corresponding register needs to be compared with the clock or calender register; if the AE bit is '1', the corresponding register is not compared, it is assumed that the register always matches the corresponding clock or calendar register. Refer to the following example:

  (1) With register 0A is set to '80', only the minute alarm and hour alarm registers need to be compared to the corresponding clock registers, ignoring the day of the week or date registers; therefore, an alarm interrupt event will be generated for each day as long as the hour and minute registers match.

  (2) Setting the AE bits in each of the 08, 09, 0A register to '1' causes an alarm interrupt event to be generated once per minute.

11.2 Fixed-Cycle Interrupt

Fixed-cycle interrupts can generate interrupt alarm events at a fixed-cycle between 244.14μs and 4095min.

11.2.1 Fixed-Cycle Interrupt Timing

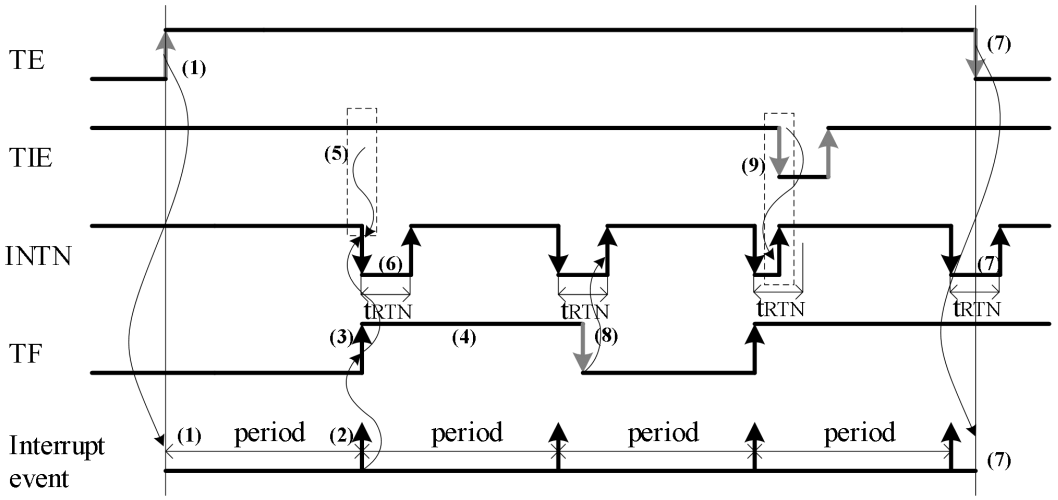


Figure 11- 2 Fixed-Cycle Interrupt Timing

(1) When '1' is written to the TE bit, the fixed-cycle counter starts counting down from the preset value.

(2) When the fixed-cycle counter counts from 001h to 000h, an interrupt event is generated; the counter is reset to a preset value and continues to the next count.

(3) When a fixed-cycle interrupt event occurs, the TF register is set to '1'.

(4) The TF register will remain at '1' until it is manually cleared to '0'.

(5) When a fixed-cycle interrupt event occurs, if TIE='1', INTN outputs a low level; if TIE='0', INTN remains in a high resistance state.

(6) INTN output a low level for tRTN length of time, after which it will automatically restore the high resistance state until the next interrupt signal output.

(7) When the TE bit is written to '0', the fixed-cycle counter stops counting and INTN outputs high resistance. (if TE is written to '0' during INTN='0', wait for tRTN time before INTN returns to the high resistance state.

(8) If TF is cleared '0' during INTN=0, the high resistance state is restored after INTN continues for tRTN time.

(9) When TIE writes '0', INTN instantly returns to the high-resistance state. If TIE is written to '1' again during tRTN, INTN returns to low level until tRTN ends.

11.2.2 Fixed-Cycle Interrupt Related Registers

Table 11- 2 Fixed-Cycle Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	TimerCounter0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C or 1C	TimerCounter1	●	●	●	●	**2048**	**1024**	**512**	**256**
0D or 1D	Extension	○	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0E or 1E	Flag	○	○	UF	**TF**	AF	○		XST
0F or 1F	Control	CSEL1	CSEL0	UIE	**TIE**	AIE	○	EN_DET	RESET

- When configuring the fixed-cycle interrupt register, it is recommended that TE and TIE should be set to '0' first to prevent unnecessary hardware interrupts from being generated during operation.
- TSEL1and TSEL0 are used to set the countdown period for fixed-cycle interrupts, and the automatic reset time of the interrupt signal on the INTN pin is related to the countdown period.

Table 11- 3 Counting Period and Automatic Reset Time for Fixed-Cycle Interrupts

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122ms
0	1	64Hz	7.8125ms
1	0	1Hz	7.8125ms
1	1	1/60Hz	7.8125ms

- Registers 0B or 1B and 0C or 1C set the default value of the counter(001h ~ FFFh). The counter generates a fixed-cycle interrupt event when it counts down to 000h with the counting period set by TSEL.
- TE is the enable control bit of fixed-cycle counter, when TE='1', the counter starts counting down; when TE='0', the counter stops counting and terminates the fixed-cycle interrupt function.
- The occurrence of a fixed-cycle interrupt event will set the TF flag position '1', which will remain '1' until it is manually cleared '0'.
- When a fixed-cycle interrupt event occurs, TIE decides whether to generate an interrupt signal output or not.(When TIE ='1', INRN ='0'; When TIE ='1', INTN = Hi-Z)

Table 11- 4 Example of a Fixed-Cycle Interrupt Cycle

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
……	……	……	……	……
2048	500ms	32s	2048s	2048min
……	……	……	……	……
4095	0.9998s	63.984s	4095s	4095min

11.3 Time Update Interruption

According to the set value, the time update interrupt generates an interrupt alarm event with a second update or a minute update.

11.3.1 Time Update Interruption Timing

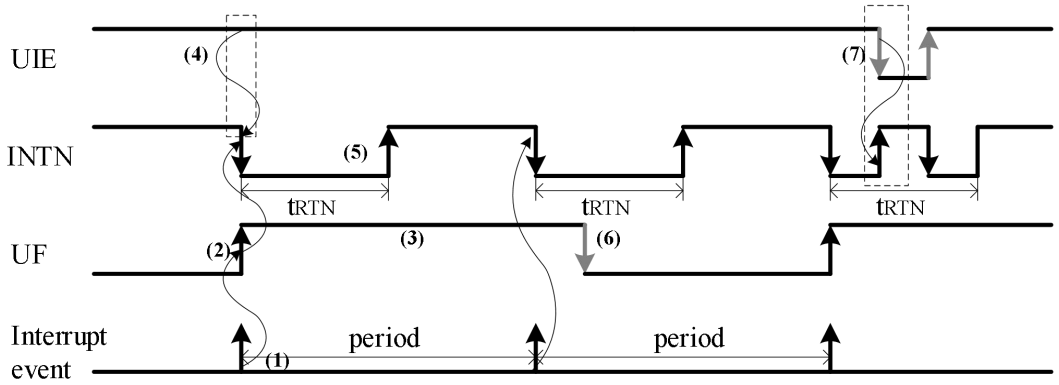


Figure 11- 3 Time Update Interrupt Timing

(1) USEL register determines whether the chip is in a second or minute update state. When the corresponding Second or Minute register updates, time update interrupt is generated.

(2) UF register is set to '1' when time update interrupt occurs.

(3) UF register will maintain '1' until it is manually cleared.

(4) When time update interrupt occurs, if UIE = '1' INTN outputs 'L', if UIE = '0' INTN maintains 'Hi-Z'.

(5) INTN outputs a low level voltage ('L') for the time length of tRTN, after which it will automatically return to 'Hi-Z' until the next interrupt signal is output.

(6) If UF is cleared (set to '0') during INTN= '0', INTN will recover to 'Hi-Z' after tRTN.

(7) IF UIE is set to '0' during INTN = '0', INTN recovers to 'Hi-Z' instantly and interrupt signal output stops. If UIE is set to '1' during tRTN again, INTN recovers to 'L' until the end of tRTN.

11.3.2 Time Update Interrupt Related Registers

Table 11- 5 Time Update Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	○	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	**UF**	TF	AF	○	○	VDET
0F or 1F	Control	CSEL1	CSEL0	**UIE**	TIE	AIE	○	EN_DET	RESET

- It is recommended to set UIE to '0' before configuring time update interrupt register in case unwanted hardware interrupt is generated during the operation.
- USEL signal is used to set whether the interrupt mode is second update or minute update.

Table 11- 6 Time Update Interrupt Mode Control

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of time update interrupt event will set UF to '1' and it maintains '1' until it is manually cleared.
- UIE determines whether or not to generate an interrupt signal output. (If UIE = '1', INTN = '0'. If UIE = '0', INTN ='Hi-Z').

12 IIC-Bus Interface

12.1 Characteristics of IIC-Bus Interface

The IIC bus supports bi-directional communications, and its signal line SDA as well as the clock line SCL need to be connected to a high level voltage through a pull-up resistor. The port connected to the IIC bus must be open-drain in order to realize multi-device line connections.

12.2 Data Transfers

One bit of data can be transmitted per SCL clock cycle. When sending data, the data on the SDA line changes during SCL is 'L'. When receiving data, valid data can be obtained from the data line SDA during SCL is 'H'.

12.3 Starting and Stopping Conditions

In the idle state, both SCL and SDA are held high. During SCL is 'H', the falling edge of SDA is used as the start condition for IIC communication, and the rising edge of SDA is used as the stopping condition for IIC communication.

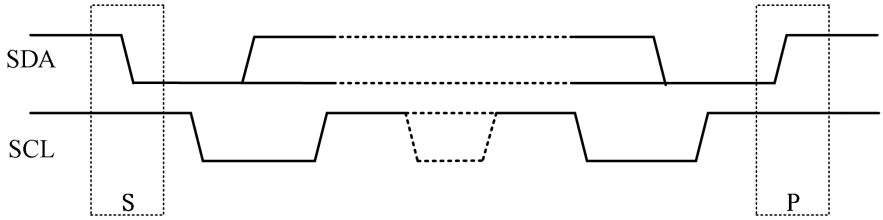


Figure 12- 1 IIC Starting and Stopping Conditions

12.4 Device Selection (Slave Address)

The IIC-Bus devices do not have any chip select or chip enable pins. The chip selection on the IIC-BUS is executed when the interface starts. The master device send the required slave address to all devices on the IIC-Bus. The slave device sends a acknowledge signal to setup communication with master device.

Slave address includes 7 bits of data ,4 bits (Group 1) + 3 bits(Group 2). The slave address of JXR231MT is “0110010”. During the communication process, the slave address and R/W bit is sent as 8bit data.

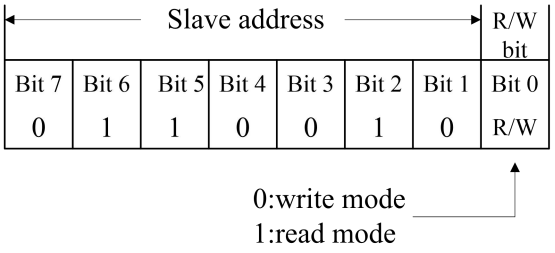


Figure 12- 2 IIC Slave Address

12.5 System Configuration

The device that will control the data transfer becomes the mater device and the devices that are controlled by the master device become the slave devices. The device that sends data is called the transmitter and the device that receives data is called the receiver.

In the JXR231MT system, CPU or other controlling device become the master device and JXR231MT itself becomes slave device. Both master and slave device can become transmitter or receiver.

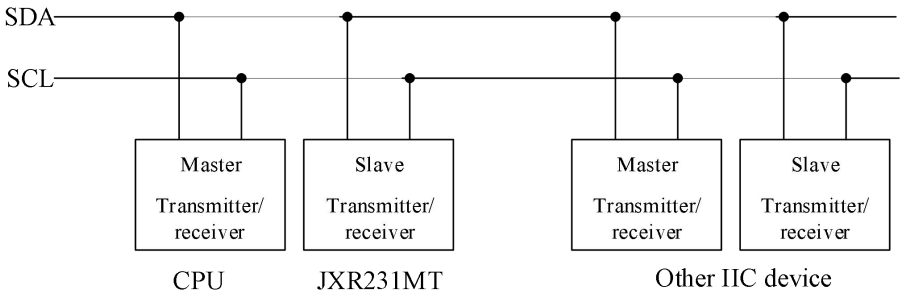


Figure 12- 3 IIC System Configuration

12.6 Acknowledge Signal

The IIC-bus has no limit on the number of bytes that can be transferred between the start and stop conditions. After each byte of data has been transferred, the transmitter releases the SDA bus and provides and SCL clock to receive an answer signal. If the receiver receives 8bit data successfully, it needs to set SDA to 0 after the end of the clock of transmitting the last 1bit data, and the transmitter will use this low level voltage as the answer signal for successful data transmission. After 1 clock cycle, the receiver releases the SDA bus and is ready to receive new data.

The IIC-bus terminates data transfer when the following conditions are met:

(1)When the master device acts as the transmitter, it sends the termination condition after receiving the answer signal from the slave device.

(2)When the master device acts as the receiver, it sends '1' as a acknowledge signal and then send a stop condition after receiving 8bit data successfully.

12.7 IIC-Bus Control

In the following sequence descriptions, it is assumed that the CPU is the master and the JXR231MT is the slave.

12.7.1 Address Specification Write Operation

Since the JXR231MT has address auto increment function, once the initial address has been specified, the JXR231MT increments the receive address each time data is transferred automatically.

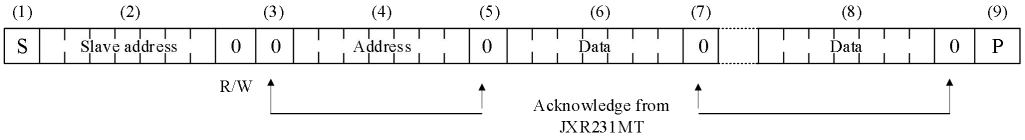


Figure 12- 4 Address Specification Write Operation

(1) CPU transfers start condition [S].

(2) CPU transfers the JXR231MT 's slave address with the R/W bit set to write mode.

(3) JXR231MT generates acknowledge signal.

(4) CPU transmits write address to JXR231MT.

(5) JXR231MT generates acknowledge signal.

(6) CPU transfers write data to the address specified at (4) above.

(7) JXR231MT generates acknowledge signal.

(8) Repeat (6) and (7) if necessary. Write addresses in JXR231MT will increase automatically.

(9) CPU transfers stop condition [P].

12.7.2 Address Specification Read Operation

After writing to the register, CPU can read the register by setting read mode.

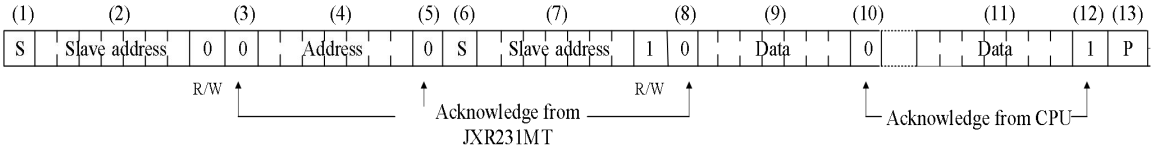


Figure 12- 5 Address Specification Read Operation

(1) CPU transfers start condition [S].

(2) CPU transfers the JXR231MT's slave address with the R/W bit set to write mode.

(3) JXR231MT generates acknowledge signal.

(4) CPU transmits read address to JXR231MT.

(5) JXR231MT generates acknowledge signal.

(6) CPU transfers start condition again.

(7) CPU transfers the JXR231MT's slave address with the R/W bit set to read mode.

(8) JXR231MT generates acknowledge signal, then CPU acts as receiver and JXR231MT acts as a transmitter.

(9) Data from address specified at (4) above is output by JXR231MT.

(10) CPU generates acknowledge signal to JXR231MT.

(11) Repeat (9) and (10) if necessary. Read addresses in JXR231MT will increase automatically.

(12) CPU generates acknowledge signal to JXR231MT..

(13) CPU transfers stop condition [P].

12.7.3 Read Operation When Address is Not Specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address +1.

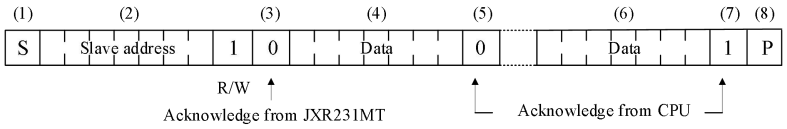


Figure 12- 6 Read Operation When Address is Not Specified

(1) (1)CPU transfers start condition [S].

(2) CPU transfers the JXR231MT's slave address with the R/W bit set to read mode.

(3) JXR231MT generates acknowledge signal, then CPU acts as receiver and JXR231MT acts as a transmitter.

(4) JXR231MT increase the read address automatically and transmit the data in the register.

(5) CPU generates acknowledge signal.

(6) Repeat (4) and (5) if necessary. Read addresses in JXR231MT will increase automatically.

(7) CPU generates acknowledge signal to JXR231MT.

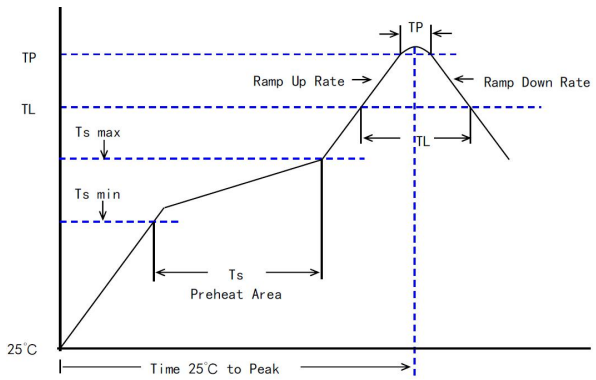
(8) CPU transfers stop condition [P].

Appendix

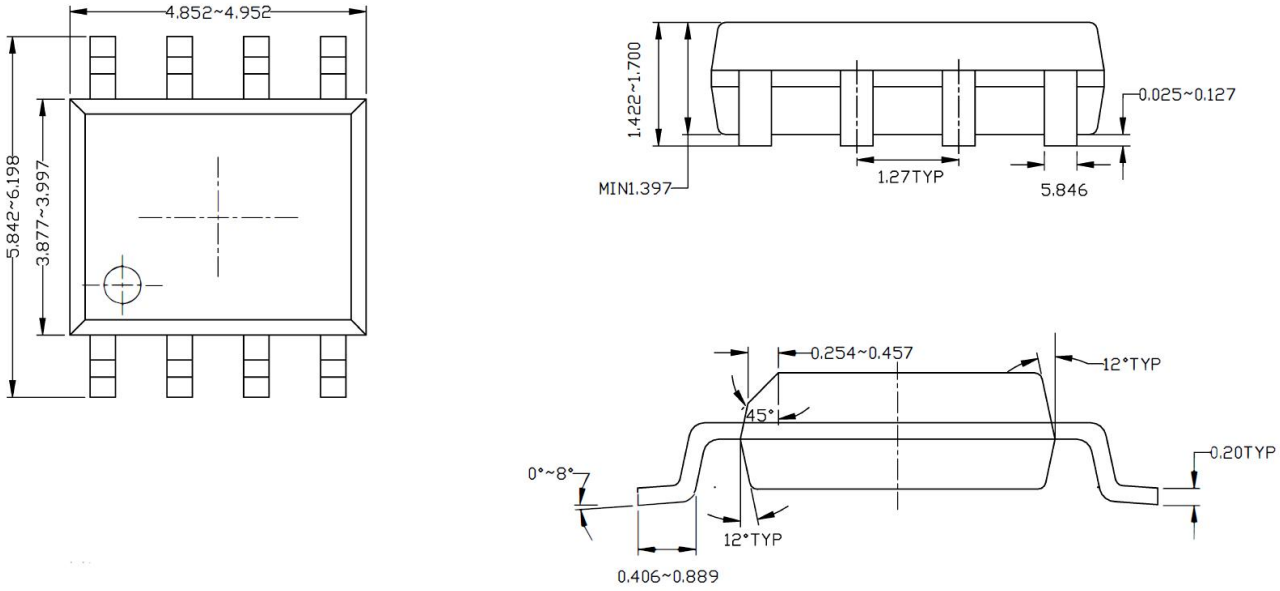
Instructions

1. Product electrostatic protection grade is HBM ±2.0kV, CDM ±2.0kV, should be prevented from electrostatic breakdown during use.
2. In the process of product use, more than 8.25 volts of power supply spike may induce latch-up effect, leading to circuit damage. At least 0.1uF decoupling capacitor should be added as close as possible to the power pin of the chip to ensure the chip's stability.
3. Since the chip is a low-power consumption IC, placing any noisy circuit components around the chip should be avoided.
4. Floating input pins may lead to increased current consumption. The chip's input pin should be connected to a fixed potential(VDD or GND) during use.
5. The chip has moisture sensitivity level of Level3. After unpacking and before welding, the workshop storage environment temperature should not exceed 30℃, and the humidity should not exceed 60%RH, and the storage time should not exceed 168 hours.
6. Peak temperature needs to be strictly controlled not to exceed 260℃ during the reflow process, otherwise the built-in crystal oscillator may be damaged, resulting in excessive clock deviation or even stopping (recommended reflow parameters are as follows).

Profiles Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Min (Ts Min)	150℃
Temperature Max (Ts Max)	200℃
Time (Ts) from (Ts Min to Ts Max)	60 ~ 120 seconds
Ramp-up rate (TL to TP)	3℃/second Max
Liquidous Temperature (TL)	217℃
Time (TL) maintained above TL	60 seconds Max
Peak/Classification Temperature (TP)	245±5℃
Time within 5℃ of actual Peak Temperature (TP)	10 seconds Max
Ramp-down rate (TP to TL)	6℃/second Max
Time 25℃ to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max



Package Size



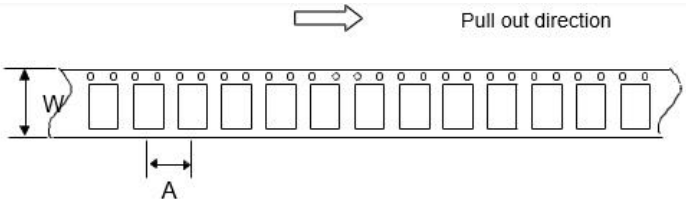
Unit：mm

Packaging Specification

Emboss Taping (TE2)

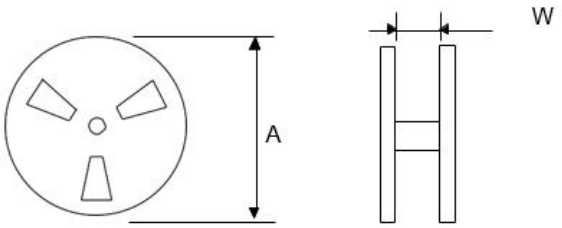
Symbol	
A	8
W	12

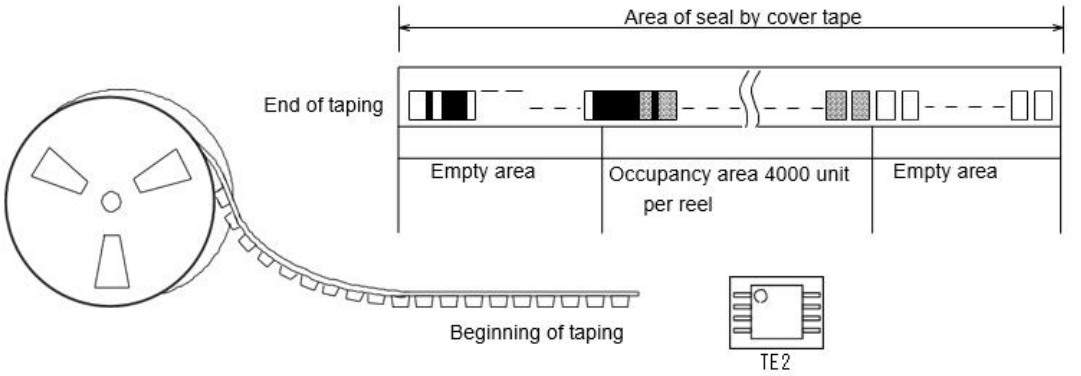
Unit : mm

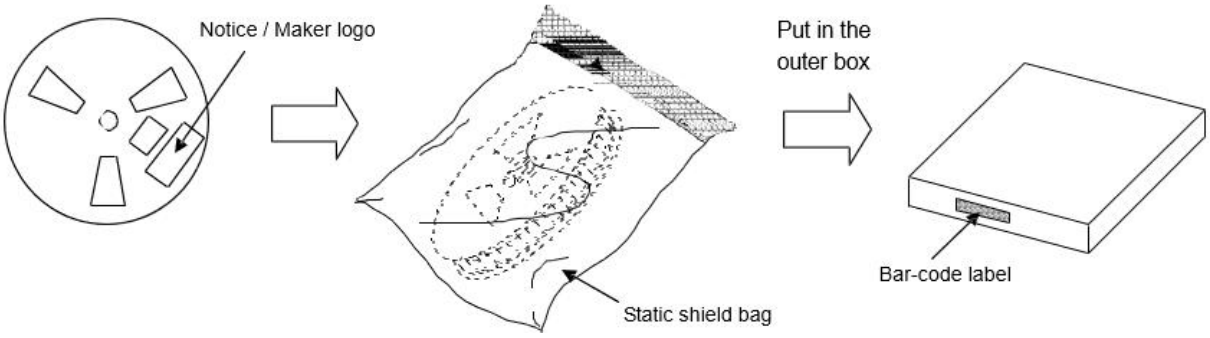


Symbol	
A	330
W	12.4
Contents	4000 pcs

Unit : mm

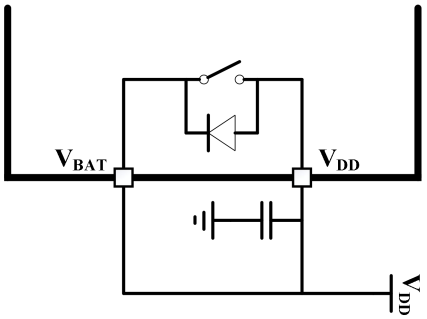




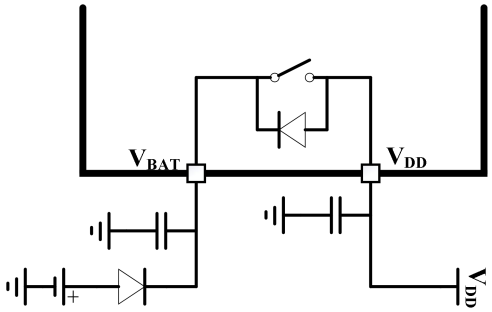


Example of Power Connection

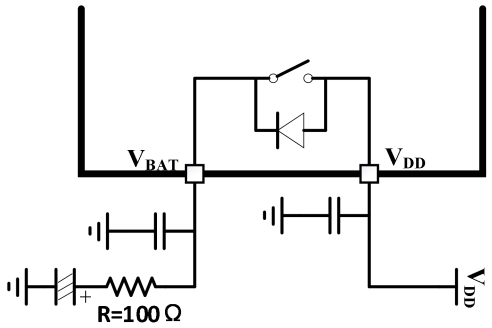
In systems that do not require a backup power supply, connect both V_{DD} and V_{BAT} to the external power supply at the same time, in witch case it is sufficient to leave the PW control register in its default configuration.



When the backup power supply uses a non-rechargeable battery, an external Schottky diode is required to prevent the battery from being charged, and in the case of a V_{DD} power-down, there will be a maximum of 1s of time where a leakage path exists from V_{BAT} to the V_{DD}.



When the backup power supply uses a rechargeable battery, it is recommended to string a resistor of about 100 Ω at the battery terminal to avoid sudden voltage change during power switching. Otherwise, in the case of a V_{DD} power-down, there will be a maximum of 1s of time where a leakage path exists from V_{BAT} to the V_{DD}.



If the rechargeable battery charging current is limited can be connected in series with a current limiting resistor of about 100 Ω ; if you do not want to have a leakage path from V_{BAT} to V_{DD}, you can connect a Schottky diode in series with the V_{DD} terminal.