JXR4020 User Manual

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catalogue

1 Summary

The JXR4020 is a low-power real-time clock chip with SPI interface and trickle charge function. It provides year/month/day/week/hour/min/second information, automatically adjusts for leap years, features AM/PM indicators, and supports both 12-hour and 24-hour operation modes.

2 Characteristic

- The real-time clock function provides information including year/month/day/week/hour /minute /second based on a 32.768kHz crystal oscillator.
- 31×8-bit general-purpose temporary RAM
- The clock circuit operates within a voltage range of 0.9V to 5.5V.
- Data transmission mode with single-byte or multi-byte (burst mode) when reading/writing clock or RAM data
- SPI 3-wire interface
- Operating voltage range: 2.0V to 5.5V
- Operating temperature range: -40℃ to 85℃
- can provide trickle charging for backup batteries
- Low current power consumption: 600nA@3.0V
- Compatible with DS1302/DS1202 pin-to-pin

3 Application Area

- telephone
- portraiture
- portable instrument
- instruments and meters

4 Structured Flowchart

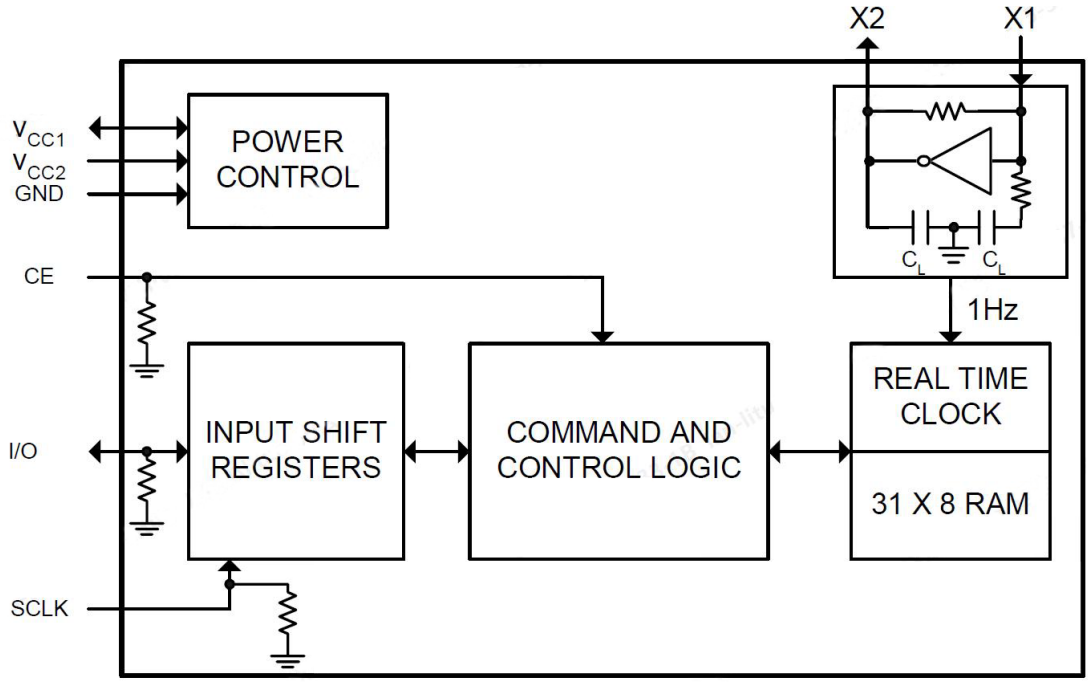


Figure 4-1 Block diagram of the JXR4020 system

5 Pin Definition

5.1 Package Form

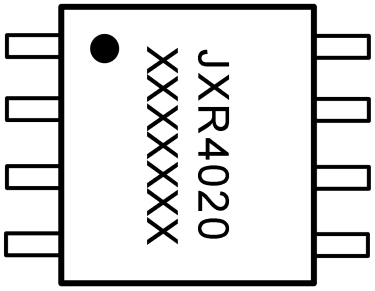


Figure 5-1 JXR4020 package form

5.2 Pin Functions

Table 5-1 JXR4020 Pin Definition

Pin No.	Pin name	Type	Description
1	VCC2	power	In a dual-power configuration, the JXR4020 draws power from the higher voltage source between VCC1 and VCC2. When VCC2 is 0.2V higher than VCC1, VCC2 supplies power to the JXR4020; when VCC1 is higher, VCC1 supplies power.
2	X1	input	The JXR4020 operates by connecting to a standard 32.768kHz quartz crystal oscillator with an external 6pF load capacitor. Alternatively, it can be driven by an external 32.768kHz oscillator, in which case X1 connects to the external oscillation signal while X2 remains unconnected.
3	X2	output	
4	GND	ground	power supply ground
5	CE	input	During read/write operations, the CE signal must remain high. This pin incorporates a built-in pull-down resistor.
6	I/O	inout	The I/O pin is a bidirectional data pin with a three-wire interface, featuring a built-in pull-down resistor.
7	SCLK	input	The SCLK pin synchronizes data operations on the serial interface, with a built-in pull-down resistor.
8	VCC1	power	The backup power supply pin maintains time and date data when the main power is unavailable; in systems with trickle charging, this pin can be connected to a rechargeable battery.

6 Absolute Maximum Rating

Table 6-1 Absolute Maximum Rated Value

Item	Symbol	Condition	Rating	Unit
Power Supply Voltage*1	Vcc	The voltage between VCC and GND	-0.5 to 6.0	V
Input voltage *1, *2	V_{IN}	CE, I/O, SCLK pins	-0.5 to VDD+0.5	V
Output voltage*1, *2	V_{OUT}	I/O pin	-0.5 to VDD+0.5	V
storage temperature	T_{STG}	Dispersed storage, unpackaged	-55 to 150	℃

*1: All electrical parameters must never exceed the maximum rated values specified in the table. Exceeding these limits may degrade performance, reduce reliability, or even cause chip failure.

*2: Here, VCC denotes the voltage range under recommended operating conditions.

7 Recommended Operating Conditions

Table 7-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
control voltage	V_{cc1}、V_{cc2}	port operation voltage	2.0	3.3	5.5	V
clock operating voltage	V_{CLK}	clock circuit operating voltage	0.9	3.3	5.5	V
service temperature	T_{OPR}	---	-40	25	85	℃

Any operation beyond the recommended range in the table may significantly compromise the chip's reliability.

8 Frequency Characteristic

Table 8-1 Frequency Characteristics

To improve timing accuracy, an external 10pF to 33pF load compensation capacitor must be added to the crystal oscillator, with the specific capacitance value determined by the application layout and the oscillator's characteristics.

Item	symbol	Condition	MIN	TYP	MAX	Unit
nominal frequency	fo			32.768(Typ)		kHz
built-in load capacitance	C_L			6		pF
load compensation capacitor	C_P		10		33	pF
take-off time	T_{STA}	T=25 ° C, VDD=2.0V ~ 5.5V, using specified crystal specifications			1.0	s
ESR driving capability	R_{ESR}	---			150	kΩ

9 Electrical Character

9.1 DC Characteristic

Table 9-1 DC Electrical Characteristics

*Unless otherwise specified, the operating conditions are: GND = 0V, V_{CC} = 2.0V ~ 5.5V, Ta = -40℃ ~ 85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
input leakage current	I_{LI}	25℃			0.1	uA
I/O leakage current	I_{LO}	25℃			0.1	uA
Input high level	V_{IH}	------	0.7*V_{CC}		V_{CC}+0.3	V
Input low level	V_{IL}	------	-0.3		0.3*V_{CC}	V
high level output	V_{OH}	V_{CC}=2.0V，I_{OH}=-0.4mA	1.7			V
		V_{CC}=5.0V，I_{OH}=-1.0mA	4.7			V
output low level	V_{OL}	V_{CC}=2.0V，I_{OH}=+1.5mA			0.4	V
		V_{CC}=5.0V，I_{OH}=+4.0mA			0.4	V
dynamic current (backup)	I_{CC1A}	V_{CC1}=2.0V，V_{CC2}=0V，CH=0*2			0.05	mA
		V_{CC1}=5.0V，V_{CC2}=0V，CH=0*2			0.1	mA
timing current (backup)	I_{CC1T}	25℃，V_{CC1}=2.0V，V_{CC2}=0V，CH=0*1		0.6	1	uA
		25℃，V_{CC1}=5.0V，V_{CC2}=0V，CH=0*1		0.7	1.2	uA
Static current (backup)	I_{CC1S}	25℃，V_{CC1}=2.0V，V_{CC2}=0V，CH=1*3		0.06	0.12	uA
		25℃，V_{CC1}=5.0V，V_{CC2}=0V，CH=1*3		0.08	0.16	uA
dynamic current	I_{CC2A}	V_{CC2}=2.0V，V_{CC1}=0V，CH=0*2			0.05	mA
		V_{CC2}=5.0V，V_{CC1}=0V，CH=0*2			0.1	mA
timing current	I_{CC2T}	25℃，V_{CC2}=2.0V，V_{CC1}=0V，CH=0*1		0.6	1	uA
		25℃，V_{CC2}=5.0V，V_{CC1}=0V，CH=0*1		0.7	1.2	uA
quiescent current	I_{CC2S}	25℃，V_{CC2}=2.0V，V_{CC1}=0V，CH=1*3		0.06	0.12	uA
		25℃，V_{CC2}=5.0V，V_{CC1}=0V，CH=1*3		0.08	0.16	uA
charging resistance of trickle current	R_1	------		2		kΩ
	R_2	------		4		
	R_3	------		8		
charge diode voltage drop of trickle current	V_{TD}	------		0.7		V
Built-in pull-down resistor		CE、I/O、SCLK pins		200		kΩ

*1. ICC1T and ICC2T represent the current power consumption with I/O open-circuit and CE/SCLK fixed grounded states.

*2. Under the conditions where ICC1A and ICC2A are open-circuit I/O, CE is high, SCLK=2MHz@VCC=5V, and SCLK=500kHz@VCC=2V, the current power consumption.

*3. ICC1S and ICC2S represent the current power consumption when CE, I/O, and SCLK are all in open-circuit state.

9.2 **AC Characteristic**

Table 9-2 AC Electrical Characteristics

*Unless otherwise specified, the operating conditions are: GND = 0V, V_{CC} = 2.0V ~ 5.5V, Ta = -40°C ~ 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Frequency	f_{SCL}	V_{CC}=2.0V			0.5	MHz
		V_{CC}=5.0V			2.0	
Data to CLK Setup	t_{DC}	V_{CC}=2.0V	200			ns
		V_{CC}=5.0V	50			
CLK to Data Hold	t_{CDH}	V_{CC}=2.0V	280			ns
		V_{CC}=5.0V	70			
CLK to Data Delay	t_{CDD}	V_{CC}=2.0V			800	ns
		V_{CC}=5.0V			200	
CLK Low Time	t_{CL}	V_{CC}=2.0V	1000			ns
		V_{CC}=5.0V	250			
CLK High Time	t_{CH}	V_{CC}=2.0V	1000			ns
		V_{CC}=5.0V	250			
CLK Rise and Fall	t_R t_F	V_{CC}=2.0V			2000	ns
		V_{CC}=5.0V			500	
CE to CLK Setup	t_{CC}	V_{CC}=2.0V	4			us
		V_{CC}=5.0V	1			
CLK to CE Hold	t_{CCH}	V_{CC}=2.0V	240			ns
		V_{CC}=5.0V	60			
CE Inactive Time	t_{CWH}	V_{CC}=2.0V	4			us
		V_{CC}=5.0V	1			
CE to I/O Input	t_{CDZ}	V_{CC}=2.0V			280	ns
		V_{CC}=5.0V			70	
		V_{CC}=5.0V			70	

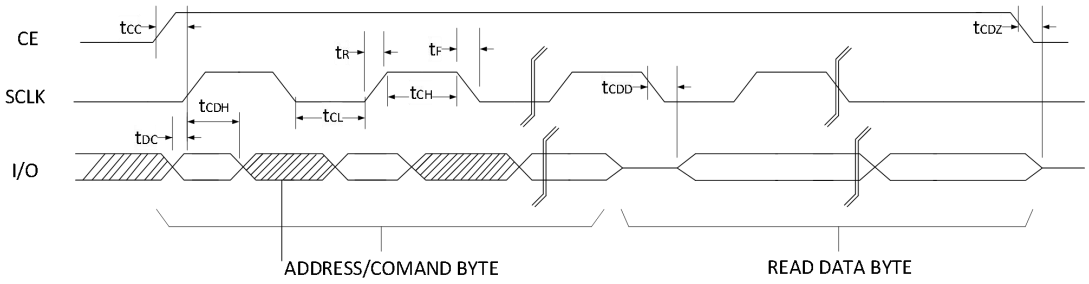


Figure 9-1 Data transfer timing diagram

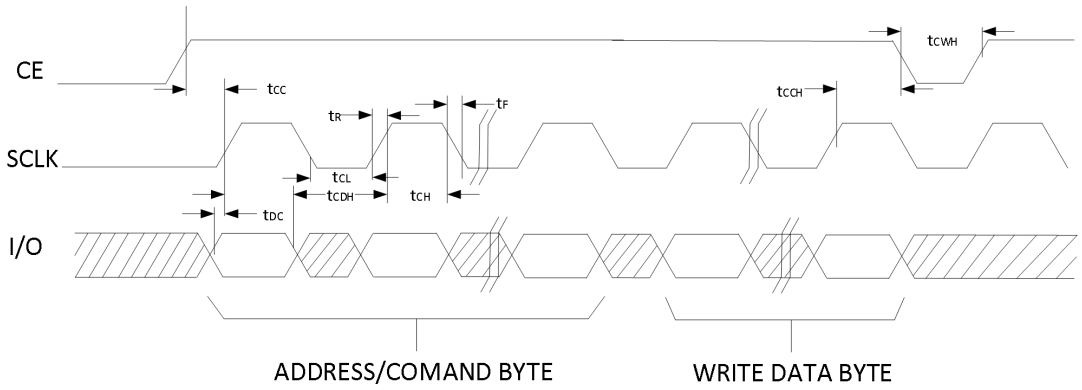


Figure 9-2 Data transfer timing diagram

10 Register

10.1 Register Table

Table 10-1 Register List

RTC

READ	WRITE	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
81h	80h	SEC	80h	CH	10 Seconds			Seconds			
83h	82h	MIN	00h	○	10 Minutes			Minutes			
85h	84h	HOUR	00h	12 / $\overline{24}$	○	$\overline{AM}$ /PM	Hour	Hour			
87h	86h	DATE	01h	○	○	10 Date		Date			
89h	88h	MONTH	01h	○	○	○	10 Month	Month			
8Bh	8Ah	DAY	01h	○	○	○	○	○	Day		
8Dh	8Ch	YEAR	00h	10 Year				Year			
8Fh	8Eh	CTRL1	00h	WP	○	○	○	○	○	○	○
91h	90h	TRICKLE CHARGE REGISTER	5Ch	TCS				DS		RS	
93h	92h	SOFT RST	00h	Write 8'h69 to execute soft reset, resetting all registers and state machine.							
95h	94h	CTRL2	0Dh	○	○	○	○	VLF	DET_EN	ADJ1	ADJ0

RTC proruption

BFh	BEh

RAM

C1h	C0h	RAM0	00h	
C3h	C2h	RAM1	00h	
C5h	C4h	RAM2	00h	
. . .	. . .	. . .	. . .	
FDh	FCh	RAM30	00h	

RAM proruption

FFh	FEh

Ensure valid values are written to the calendar and clock registers; otherwise, the chip cannot perform proper timing operations.

*The register bits marked with ○ are read-only, and their value is 1'b0.

10.2 Register Specification

10.2.1 RTC register

- Data format

RTC register data is in BCD code format. For example, the value '0101 1001' in the second register indicates the current time is 59 seconds.

- CH

The bit7 of the second register is designated as the clock pause register. When this bit is set to 1, the clock oscillator pauses, and the JXR4020 enters a low-power standby mode with a leakage current below 100nA. When this bit is set to 0, the clock resumes operation.

- $12 / \overline{24}$

The JXR4020 operates in either 12-hour or 24-hour mode, with bit7 of the timer register serving as the mode selection bit. Setting this bit to 1 activates the 12-hour mode, while setting it to 0 enables the 24-hour mode.

- $\overline{\text{AM}}/\text{PM}$

12-hour timekeeping: A 0 in this bit indicates morning, while a 1 indicates afternoon.

24-hour timer: This bit is the most significant bit of the hour count.

- Day register

The Day register increments at midnight. Its value can be customized by the customer, but must be consecutive (for example, 1 for Sunday and 2 for Monday).

- Year register

The year register's value ranges from 00 to 99, resetting to 00 after 99. A year is considered a leap year if its value is divisible by 4. The calendar's valid period spans from 2000 to 2099.

10.2.2 Control register

CTRL1			
Bit	Symbol	Value	Description
7	Write Protection Flag (WP)	1	Write operations on any register are prohibited
		0	Supports register write operations
6 ~ 0	-	0	Read-only bit, always set to 0 during read

- WP position

The write protection bit (bit7) must be set to 0 before any write operation on the RTC or RAM. When bit7 is 1, the write protection bit blocks all write operations to any register.

CTRL2			
Bit	Symbol	Value	Description
7 ~ 4	-	0	Read-only bit, always set to 0 during read
3	VLF	0	The clock chip has been running continuously after setup without any abnormal stoppage events.
		1	The clock chip experienced an out-of-sync event. The current time is not reliable.
2	DET_EN	0	Disable anti-vibration detection
		1	Enable stoppage detection
1 ~ 0	ADJ	0	fine-tuning chip power consumption

- VLF bit

Stoppage Detection Flag. When CH=0, the crystal oscillator operates normally. If the oscillator stops oscillating and the clock circuit fails to function properly, this flag is set to 1. It remains at 1 until manually reset to 0, and manual setting is prohibited. The flag defaults to 1 upon power-up, indicating inaccurate timing and requiring time configuration. After setting the time, the VLF flag can be reset to 0 via SPI, and it stays at 0 until the oscillator stops oscillating again. When CH=1, the clock is paused, the stoppage detection function is disabled, and the VLF flag remains at 0.

- ADJ position

The clock chip's power regulation bit adjusts the chip's current power consumption by modifying the control bit's state. When the external crystal oscillator (ESR) is low, the chip power can be appropriately reduced. Refer to Table 10-2 for specific adjustment details.

Table 10-2 Power Consumption Adjustment Control Table

ADJ1	ADJ0	Current Consumption
0	0	650 nA
0	1	600 nA *Default
1	0	550nA
1	1	500nA

10.2.3 Trickle Charge register

This register governs the trickle charging function of the JXR4020. The trickle charging select bit (TCS) controls the trickle charger's activation. To prevent accidental activation, only the 1010 data mode enables the trickle charger, while all other modes disable it (including during the JXR4020's power-up).

The diode selection (DS) bit determines the number of diodes between VCC2 and VCC1. When the DS bit is 00 or 11, the trickle charger is disabled.

The RS bit (Resistor Selection Bit) determines the resistance level between VCC2 and VCC1. Table 10-3 shows the selection of charging resistance and diode.

Table 10-3 Drain Current Charging Resistance and Diode Selection Table

TCS BIT7	TCS BIT6	TCS BIT5	TCS BIT4	DS BIT3	DS BIT2	RS BIT1	RS BIT0	FUNCTION
×	×	×	×	×	×	0	0	Disabled
×	×	×	×	0	0	×	×	Disabled
×	×	×	×	1	1	×	×	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	2 Diode, 2kΩ
1	0	1	0	1	0	1	0	2 Diode, 4kΩ
1	0	1	0	1	0	1	1	2 Diode, 8kΩ
0	1	0	1	1	1	0	0	Initial power-on state

In this 5V system, the power supply is connected to VCC2, with a supercapacitor linked to VCC1 as a backup power source. The trickle charger is enabled, and a diode and resistor R1 are connected between VCC2 and VCC1. The maximum current (IMAX) is calculated as follows:

$$I_{MAX} = (5.0V - Vdiodedrop)/R_1 \approx (5.0V - 0.7V)/2k\Omega \approx 2.2mA$$

As the supercapacitor charges continuously, the voltage drop between VCC2 and VCC1 decreases, resulting in a reduction of the charging current.

10.2.4 RAM register

Static RAM is addressed in byte continuous 31in RAM address space, and can store 248-bit data.

11 SPI BI

11.1 Characteristics of SPI Bus

SPI is a bidirectional communication interface that uses three parallel lines for data transfer: a clock line (SCLK), an input/output line (I/O), and an enable line.

11.2 CW

When transmitting data, you must follow a specific command word format, as shown in the table below.

7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

The command word initiates each data transfer, where the MSB (bit 7) must be logic 1. A bit 0 disables write operations to the JXR4020. Bit 6 controls clock/calender data when logic 0, and RAM data when logic 1. Bits 1-5 designate input/output registers. The LSB (bit 0) enables write operations (output) when logic 0 and read operations when logic 1. Command word formatting follows a bottom-up transmission sequence, starting with the LSB (bit 0).

11.3 CE clock control

CE input mainly realizes two functions: first, CE enable control logic for the read and write of address and command sequence shift register; second, CE signal is the termination signal for single byte and multi-byte read and write operation.

Input data is valid on the rising edge of SCLK, and output data is valid on the falling edge. If the CE input is low, data transmission stops.

11.4 SPI bus control

This section describes the SPI bus communication timing when the CPU acts as the master device and the JXR4020 as the slave device.

11.4.1 single byte write operation

The CPU can write the register data by setting the write mode.

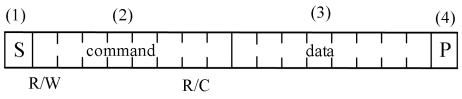


Figure 11-1 specifies the address write operation

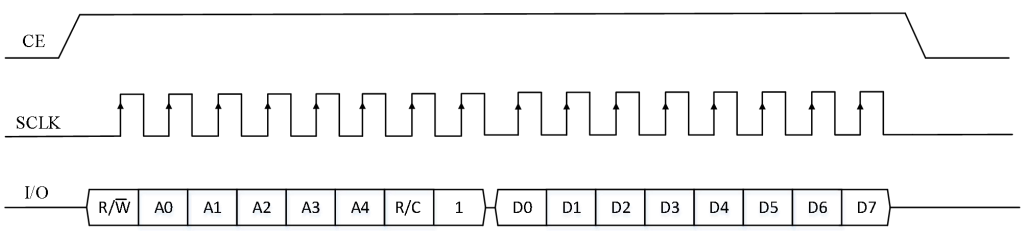


Figure 11-2 Schematic diagram of single-byte write timing for specified address

(1) Initial condition [S]: The CPU pulls the CE line high to initiate data communication.

(2) The CPU sends the specified register input from the JXR4020 and sets the write mode via the R/W bit, then selects RAM/RTC data for writing through the R/C bit.

(3) The falling edge of eight SCLK cycles outputs one byte of data (bit 0 transmission occurs on the first falling edge after the command word is written).

(4) Termination condition [P]: The CPU pulls the CE line low to stop data communication.

11.4.2 single byte read operation

After writing to the register, the CPU can read the register data by setting the read mode.

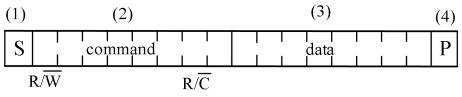


Figure 11-3 Single-byte read operation at specified address

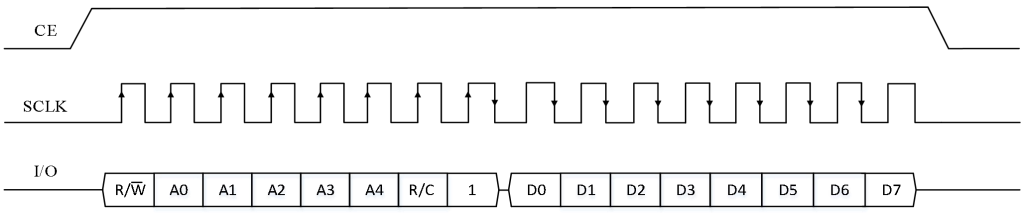


Figure 11-4 Schematic diagram of single-byte read timing for specified address

(1) Initial condition [S]: The CPU pulls the CE line high to initiate data communication.

(2) The CPU sends the specified register input from the JXR4020 and sets it to read mode via the Read/Write (R/W) bit, then selects to write RAM/RTC data through the Read/Write (R/C) bit.

(3) Input one byte of data during the rising edge of eight SCLK cycles

(4) Termination condition [P]: The CPU pulls the CE line low to stop data communication. The PU retransmits the initial condition.

11.4.3 burst read/write mode

The burst read/write mode can be configured for clock, calendar, or RAM registers. As mentioned earlier, bit 6 specifies the clock or RAM, while bit 0 controls read/write operations.

In pulse-string mode, the first eight registers must sequentially write the data to be sent. However, when writing to RAM in pulse-string mode, there is no need to write all 31 bytes of data. Regardless of the number of bytes written, each byte will be written to RAM.

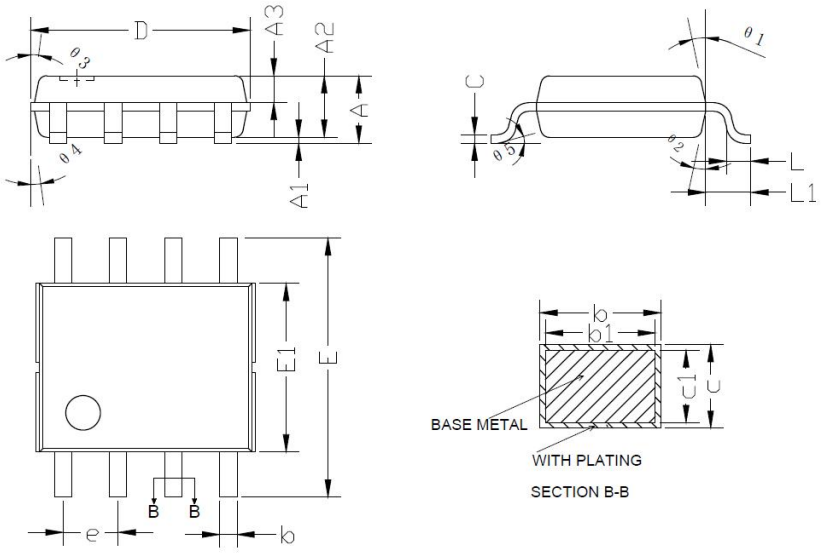
Appendix

direction for use

- The product features an electrostatic protection rating of HBM ±2.0kV and CDM ±1.0kV. During operation, precautions must be taken to prevent electrostatic discharge.
- During operation, power spikes exceeding 8.25V may trigger latch-up effects and circuit damage. To ensure stable chip operation, install a decoupling capacitor (minimum 0.1uF) near the clock chip's power pin.
- Because the clock chip is a low power integrated circuit, it is necessary to avoid placing any high noise components around the clock chip.
- Floating input pins on a chip may increase current power consumption. During operation, the input pins should be connected to a fixed potential (VDD or VSS).
- The chip's humidity sensitivity level is Level 3. From unpacking to soldering onto the board, the workshop storage environment must maintain a temperature and humidity of no more than 30°C and 60% RH, respectively, with a storage duration not exceeding 168 hours. If these storage conditions are exceeded, the chip must undergo baking treatment before SMT mounting, with baking conditions set at 125°C for 16 hours or 60°C for 48 hours.

Encapsulation size

SOP8: 8-pin plastic encapsulation, body width 3.9mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.65
A1	0.10	--	0.25
A2	1.40	1.42	1.50
A3	0.57	0.62	0.67
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.90	6.00	6.20
E1	3.85	3.90	4.00
e	1.27(BSC)		
L	0.50	0.60	0.70
L1	1.05(BSC)		
θ1	9°	~	15°
θ2	9°	~	15°
θ3	8°	~	14°
θ4	8°	~	14°
θ5	0°	~	6°

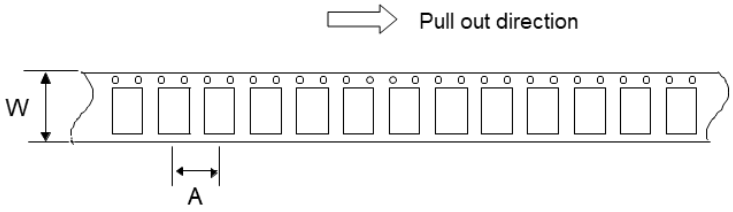
packing specifications

SOP8

SOP Emboss Taping (TL)

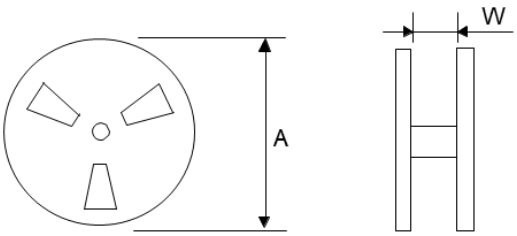
Symbol	SOP8
A	8
W	12

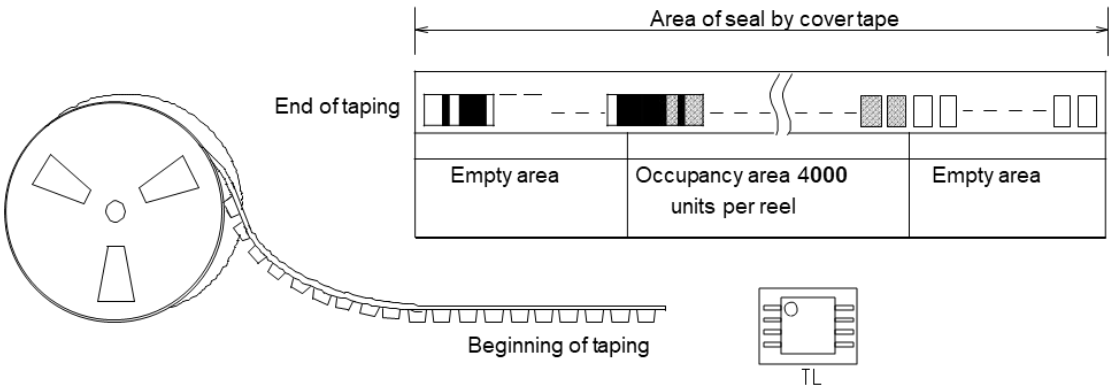
Unit : mm

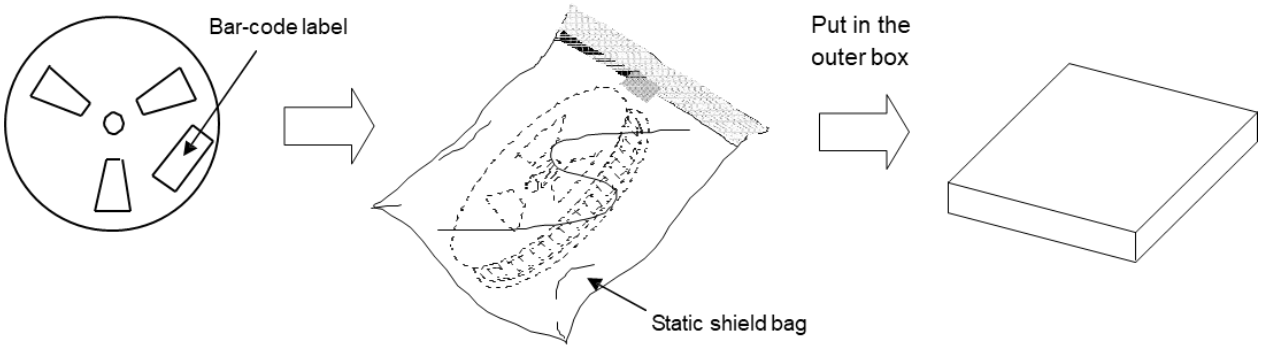


Symbol	SOP8
A	330
W	12

Unit : mm







Order Information

product name	material number	encapsulation form	Packaging format	Minimum order quantity
JXR4020	OSC0D40200001000	SOP8	13-inch reel	4000

Product Label Description