JXR271T-GA User Manual

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catalogue

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1 summary

The JXR271T-GA is a high-precision automotive-grade real-time clock chip with an IIC interface and an integrated 32.768kHz temperature-compensated crystal oscillator (D-TCXO). It features automatic leap year correction and provides timing alarm interrupts, fixed-period interrupts, time update interrupts, as well as clock outputs at 32.768kHz, 1024Hz, 32Hz, and 1Hz.

The chip has passed the AEC-Q200 automotive-grade certification, with a temperature range of-45℃ to 125℃. It delivers ultra-precise clock outputs within the-45℃ to 105℃ range. Featuring timestamp functionality, it can be configured to trigger based on external or internal events, supporting up to 8 timestamp groups that record event types and timestamps.

2 characteristic

- Built-in high-precision 32.768kHz D-TCXO
- ms precision
- Supports high-speed IIC bus protocol (400kHz)
- The operating temperature range covers-45℃ to 125℃
- High Frequency Stability (UA):
- 25℃: <1.0 ppm; (daily timing error less than 0.086 s)
- 0℃ to 50℃: <1.5 ppm; (daily timing error less than 0.130 s)
- -45℃ to 85℃: <3.0 ppm; (daily timing error less than 0.259 s)
- 85℃ to 105℃: <5.0 ppm; (daily timing error less than 0.432 s)
- Time alarm interrupt function (settable: day, week, hour, minute)
- Fixed cycle interrupt function
- Time update interrupt function
- Clock output with enable control at 32.768kHz/1024Hz/32Hz/1Hz
- The calendar range supports years from 2000 to 2099 and automatically adjusts for leap years.
- The operating voltage range of the temperature compensation circuit is 2.2V to 5.5V.
- The clock circuit operates within a voltage range of 1.0V to 5.5V.
- Built-in timestamp feature, triggered by external or internal events
- Built-in 64-byte user RAM (when timestamp is not in use)
- Low current power consumption: 0.9μA@3V (Typ)
- Certified to AEC-Q200 automotive-grade standards

3 structure flowchart
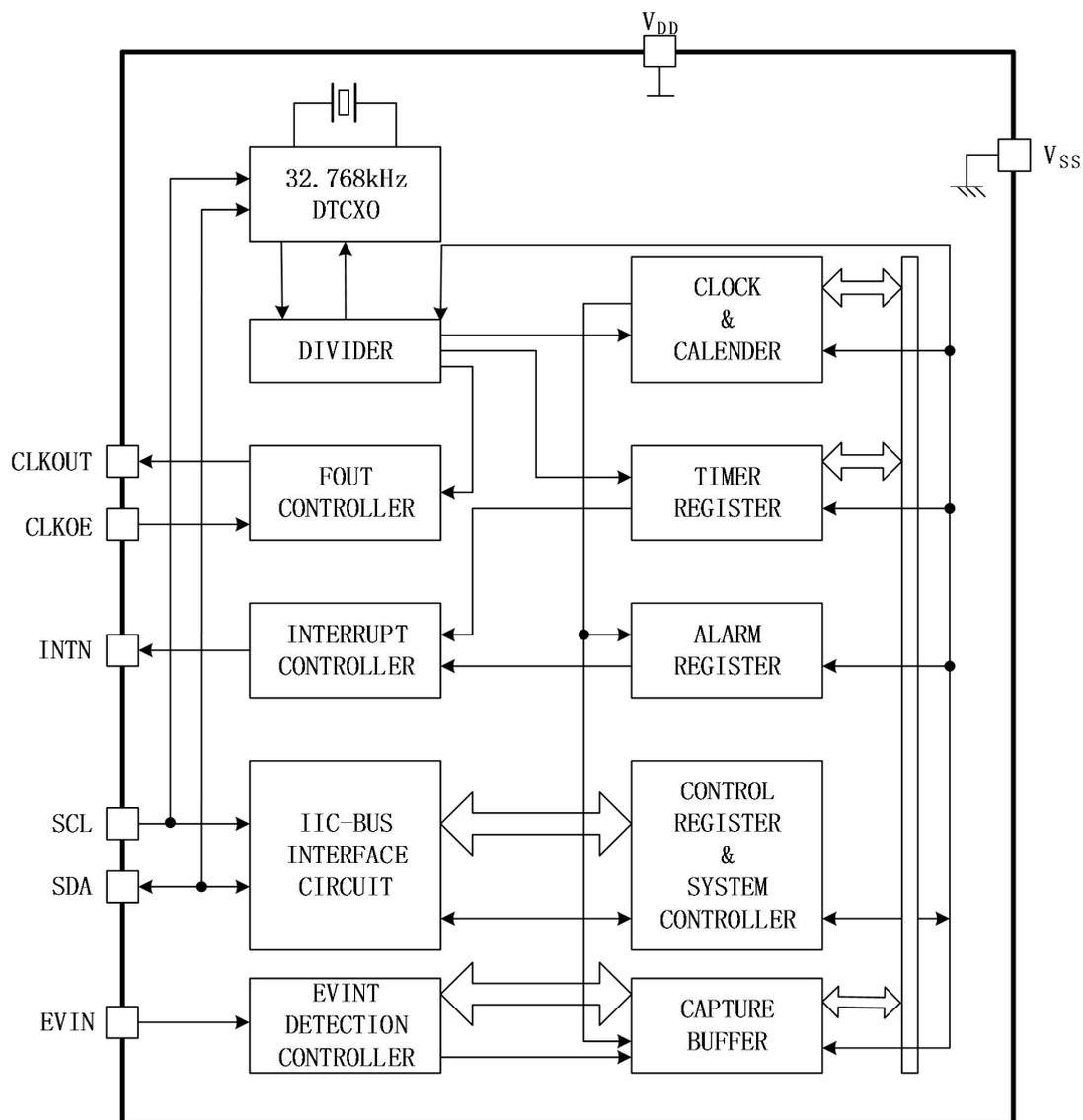
Figure 3-1 Block diagram of the JXR271T-GA system

4　Pin definition

4.1 **package form**
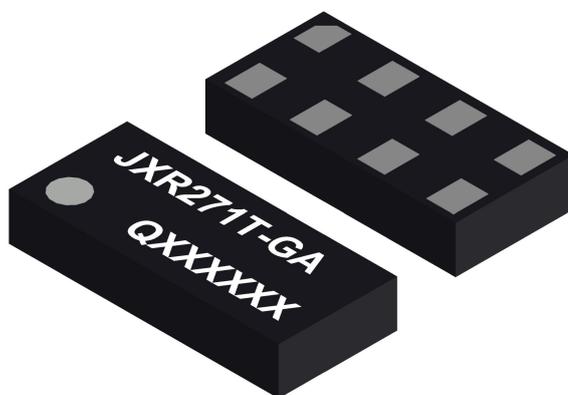
Figure 4-1 JXR271T-GA package form

4.2 **Pin functions**

Table 4-1 JXR271T-GA Pin Definition

Pin name	I/O	Function
1. SDA	INOUT	IIC bus communication data transmission end, N-channel open drain output
2. CLKOUT	OUTPUT	The 32.768kHz frequency output port is controlled by CLKOE. When CLKOE is set to '1', it outputs a 32.768kHz clock signal; when CLKOE is '0', it outputs a high-impedance state.
3. VDD	POWER	main power source
4. CLKOE	INPUT	CLKOUT is enabled for frequency output when CLKOE is set to '1'.
5. VSS	GROUND	power supply ground terminal
6. INTN	OUTPUT	Interrupt output port, N-channel open drain output
7. EVIN	INPUT	The external event trigger timestamp interface can be configured for high-pulse or low-pulse trigger mode.
8. SCL	INPUT	IIC bus communication serial clock input

5 absolute maximum rating

<p align="center">Table 5-1 Absolute Maximum Rated Value</p>

Item	Symbol	Condition	Rating	Unit
Power Supply Voltage[*1]	V_{DD}	Voltage between V_{DD} and V_{SS}	-0.5 to 6	V
Input voltage [*1, *2]	V_{IN}	CLKOE, SCL, SDA , EVIN pins	-0.5 to V_{DD} + 0.5	V
Output voltage[*1, *2]	V_{OUT}	CLKOUT, SDA, INTN pins	-0.5 to V_{DD} + 0.5	V
storage temperature	T_{STG}	Dispersed storage, unpackaged	-55 to 125	°C

*1: All electrical parameters must never exceed the maximum rated values specified in the table. Exceeding these limits may degrade performance, reduce reliability, or even cause chip failure.

*2: V_{DD} denotes the recommended operating voltage range.

6 Recommended operating conditions

<p align="center">Table 6-1 Recommended Operating Conditions</p>

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
control voltage	V_{DD}	interface voltage	1.5	3.0	5.5	V
temperature compensation voltage	V_{TEM}	working voltage of Temperature Compensation circuit	2.2	3.0	5.5	V
clock operating voltage	V_{CLK}	operating voltage of oscillator module	1.0	3.0	5.5	V
temperature compensation range	V_{COMP}	Range of Temperature Compensation	-45	25	105	°C
service temperature	T_{OPR}	---	-45	25	125	°C

Any operation beyond the recommended parameters in the table may significantly compromise the chip's reliability.

7   frequency characteristic

Table 7-1 Frequency Characteristics

Item	symbol	Condition		MIN	MAX	Unit
frequency stability	$\Delta f/f$	Ta = 25 ℃, V_{DD} = 3.0V		-1.0	+1.0	×10^{-6}
		Ta = 0 ℃ ~ 50 ℃, V_{DD} = 3.0V	UA	-1.5	+1.5	
			UB	-3.0	+3.0	
		Ta = -45 ℃ ~ 85 ℃, V_{DD} = 3.0V	UA	-3.0	+3.0	
			UB	-5.0	+5.0	
		Ta = 85 ℃ ~ 105 ℃, V_{DD} = 3.0V	UA	-5.0	+5.0	
			UB	-8.0	+8.0	
		Ta = 105 ℃ ~ 125 ℃, V_{DD} = 3.0V		-80.0	+10.0	
voltage coefficient	$\Delta f/f/V$	Ta = 25 ℃, V_{DD} = 2.2V ~ 5.5V		-1.0	+1.0	×10^{-6}/V
take-off time	T_{STA}	Ta = 25 ℃, V_{DD} = 1.5V ~ 5.5V			1.0	s
		Ta = -40 ℃ ~ 85 ℃, V_{DD} = 1.5V ~ 5.5V			2.0	
Aging	fa	Ta = 25 ℃, V_{DD} = 3.0V, first year		-1.0	+1.0	×10^{-6}/year

8   electrical character

8.1 **DC characteristic**

Table 8-1 DC Electrical Characteristics

Unless otherwise specified, the operating conditions are: V_{SS} = 0V, V_{DD} = 1.5V to 5.5V, and Ta = -40°C to 85°C.

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
current power dissipation	I_{DD1}	CLKOE = V_{SS} CLKOUT = '0'	V_{DD} = 5V		1.2	3.0	μA
	I_{DD2}		V_{DD} = 3V		0.9	2.0	
current power dissipation	I_{DD3}	CLKOE = V_{DD} CLKOUT=32.768kHz CL = 0pF	V_{DD} = 5V		3.6		μA
	I_{DD4}		V_{DD} = 3V		2.9		
current power dissipation	I_{DD5}	CLKOE = V_{DD} CLKOUT = 32.768kHz CL = 30pF	V_{DD} = 5V		7.5		μA
	I_{DD6}		V_{DD} = 3V		6.2		
current power dissipation	I_{DD7}	During IIC communication, V_{DD} = 5V				5.0	μA
high input level	V_{IH}	CLKOE, SCL, SDA, EVIN pins	V_{DD} = 2.2V ~ 5.5V	$0.7*V_{DD}$		V_{DD}+0.3	V
low input level	V_{IL}	CLKOE, SCL, SDA, EVIN pins	V_{DD} = 2.2V ~ 5.5V	-0.3		$0.3*V_{DD}$	V
high output level	V_{OH}	CLKOUT pin	I_{OH} = -1mA	V_{DD}-0.3		V_{DD}	V
low output level	V_{OL}	CLKOUT, INTN pins	I_{OL} = 1mA	V_{SS}		V_{SS}+0.3	V
		SDA pin	$V_{DD} \geq 2V$ I_{OL} = 3mA	V_{SS}		V_{SS}+0.3	V
input leakage current	I_{LK}	CLKOE, SCL, SDA, EVIN, V_{IN}=V_{DD} or V_{SS}		-0.1		0.1	μA
output leakage current	I_{OZ}	INTN, CLKOUT, SDA, V_{IN}=V_{DD} or V_{SS}		-0.1		0.1	μA

8.2 **AC characteristic**

Table 8-2 AC Electrical Characteristics

Unless otherwise specified, the operating conditions are: $V_{SS} = 0V$, $V_{DD} = 1.5V$ to $5.5V$, and Ta = -40°C to 85°C.

Item	Symbol	Condition	Standard Mode			Fast Mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	---			100			400	kHz
initial condition establishment time	$t_{SU;STA}$	---	4.7			0.6			μs
initial condition holding time	$t_{HD;STA}$	---	4.0			0.6			μs
data transfer setup time	$t_{SU;DAT}$	---	250			100			ns
data transmission hold time	$t_{HD;DAT}$	---	0			0			ns
Termination condition establishment time	$t_{SU;STO}$	---	4.0			0.6			μs
bus idle time	t_{BUF}	Between termination and initial conditions	4.7			1.3			μs
SCL low level time	t_{LOW}	---	4.0			1.0			μs
SCL high level time	t_{HIGH}	---	4.0			1.0			μs
SCL, SDA rise time	t_r	---			1.0			0.3	μs
SCL, SDA decline time	t_f	---			0.3			0.3	μs
bus spike duration	t_{SP}	---			50			50	ns
FOUT output duty cycle	Duty	Calculate the output as 50% of V_{DD}.	40	50	60	40	50	60	%
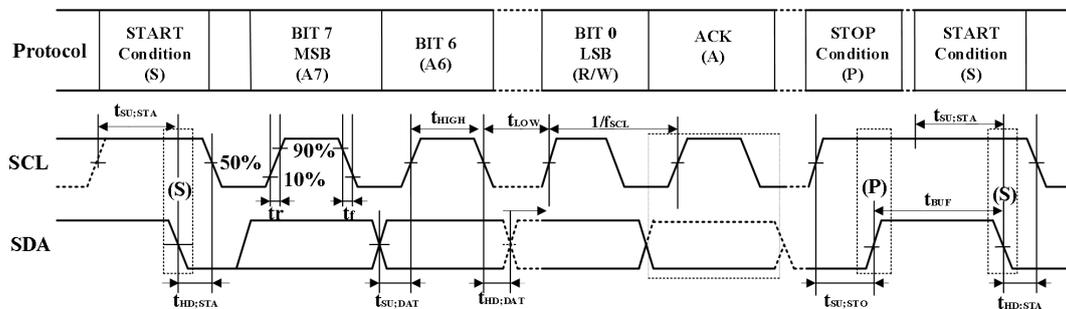
Figure 8-1 IIC timing diagram

The IIC data transfer occurs between the start and stop conditions, and must be completed within 0.95 seconds.
If this time limit is exceeded, the IIC bus will be reset by the internal timer.

9 register

9.1 register table

Table 9-1 Register List

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70	MSEC[9:8]	8'h00	○	○	○	○	○	○	512	256
71	MSEC[7:0]	8'h00	128	64	32	16	8	4	2	1
00 or 10	SEC	8'h00	○	40	20	10	8	4	2	1
01 or 11	MIN	8'h00	○	40	20	10	8	4	2	1
02 or 12	HOUR	8'h00	○	○	20	10	8	4	2	1
03 or 13	WEEK	8'h40	○	6	5	4	3	2	1	0
04 or 14	DAY	8'h01	○	○	20	10	8	4	2	1
05 or 15	MONTH	8'h01	○	○	○	10	8	4	2	1
06 or 16	YEAR	8'h00	80	40	20	10	8	4	2	1
07	RAM	8'h00	●	●	●	●	●	●	●	●
08	MIN Alarm	8'h00	AE	40	20	10	8	4	2	1
09	HOUR Alarm	8'h00	AE	●	20	10	8	4	2	1
0A	WEEK Alarm	8'h00	AE	6	5	4	3	2	1	0
	DAY Alarm			●	20	10	8	4	2	1
0B or 1B	TimerCounter0	8'h00	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	8'h00	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	8'h02	ETS	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8'h01	○	○	UF	TF	AF	EVF	○	XST
0F or 1F	Control	8'h42	CSEL1	CSEL0	UIE	TIE	AIE	EIE	EN_DET	RESET
1A	Offset	8'h00	○	○	○	○	OFS3	OFS2	OFS1	OFS0
20 ~ 28	Time Stamp	8'h00	Time Stamp 1/1024s → Year							
29	Stamp Status	8'h00	EVTP1	EVTP0	○	○	○	○	SXST	○
2A	EVIN Setting	8'h00	EHL	ET1	ET0	PDN	○	PU	OVW	○
2B	Command Trigger Ctrl	8'h00	○	○	○	○	○	○	○	COMTG
2C	Command Trigger	8'h00								
2D	TS Control0	8'h00	○	○	○	○	○	EISEL	TSCLR	TSRAM
2E	TS Control1	8'h00	○	○	PRCT1	PRCT0	○	○	○	EXST
2F	TS Control2	8'h2f	○	○	1'b1	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0
30 ~ 6F	TS RAM	8'h00								

Ensure valid values are written to the calendar and clock registers; otherwise, the chip cannot perform proper timing operations.

*Bits marked as ○ are read-only, with a default value of '0' and write access disabled. ●-marked bits support RAM read/write operations.

If the alarm interrupt function is not enabled (AIE = '0'), registers 8 through A can be used as RAM.

If no fixed period interrupt function is configured (TE = TIE = '0'), registers 0B or 1B,0C or 1C can be used as RAM.

The UF, TF, AF, and XST bits can only be set to '0'.

During power-up, the CSEL0 bit is set to '1', while the FSEL1, FSEL0, CSEL1, UIE, TIE, and AIE bits are set to '0'.

* MSEC[9:8] and MSEC[7:0] are read-only registers.

9.2 **register specification**

9.2.1 **Clock and calendar registers (registers 00－06 or 10－16)**

- Data format

All data except the week register (register 3) is in BCD code format. For example, the value "0101 1001" in the second register indicates the current time is 59 seconds.

The timekeeping mode is fixed to 24-hour system.

- Year Register and Leap Year

The year register's value ranges from 00 to 99, resetting to 00 after 99. A year is considered a leap year if its value is divisible by 4. The calendar's valid period spans from 2000 to 2099.

- week register

The week register has 7 valid bits (bit0 to bit6), each representing a day of the week from Monday to Sunday. Therefore, only one bit can be set to '1' in this register.

Table 9-2 Week Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

9.2.2 **Millisecond registers (registers 70,71)**

These two registers are read-only and cannot be written to, designed to provide millisecond-level timing for users, delivering clock accuracy beyond the second. The millisecond registers share 10 valid bits (Register 70 for the upper 2 bits, Register 71 for the lower 8 bits), with a timing precision of 1/1024 second.

When the user configures the second register, registers 70 and 71 are automatically reset to '0', and the timer restarts from 0ms.

9.2.3 **alarm register (register 08 to 0A)**

The alarm can be configured to occur at X hour X minute on X day of each week (weekly alarm mode) or at X hour X minute on X day of each month (daily alarm mode). The alarm mode can be set through the WADA bit in register 0D or 1D.

Each alarm register contains an AE (Alarm Enable) bit (bit7). When the AE bit of a register is '0', its set value must be compared with the corresponding timer register. If the values match, an alarm interrupt is triggered. If the AE bit is '1', the corresponding alarm register value is ignored, meaning no comparison is required with the timer register, and the register value is always considered identical to the timer register value.

When the week alarm mode is selected, multiple days of the week can be chosen simultaneously, meaning that several bits (bit0 to bit6) in the WEEK ALARM function of register 0A or 1A can be set to '1'. Refer to Table 9-3 for the corresponding relationships under the week alarm mode.

Table 9-3 Week Alarm Mode Register A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0A	Week Alarm	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

9.2.4 Fixed period counter control register (register 0B or 1B,0C or 1C)

These two registers store preset countdown values for fixed-period interrupts. When their values transition from 001h to 000h, a fixed-period interrupt occurs: TF is set to '1' and INTN outputs a low level (if TIE is '1'). Subsequently, the 0B or 1B,0C or 1C registers reset to their preset values, restarting the countdown process.

9.2.5 Control registers and flag registers (registers 0D to 0F or 1D to 1F)

- ETS site

The EVIN trigger timestamp enable bit. Set to '1' to enable EVIN trigger timestamps, set to '0' to disable the function.

- WADA position

Alarm interrupt mode selection bit: set to '1' for daily alarm mode, set to '0' for weekly alarm mode.

- USEL bit

Sets the period for time update interrupts; this bit defaults to '0' when the chip is powered on.

Table 9-4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE position

When the position is '1', the counter for fixed-period interrupts starts counting down; when it is '0', the countdown stops.

- FSEL bit

This parameter sets the output frequency of the CLKOUT port, with specific configurations as shown in Table 9-5. The default value is '00' after the chip is powered on.

Table 9-5 CLKOUT Output Frequency Selection

FSEL1	FSEL0	CLKOUT frequency
0	0	32.768kHz *Default
0	1	1024Hz
1	0	32Hz
1	1	1Hz

- TSEL bit

Sets the count period for fixed periodic interrupts.

Table 9-6 Fixed Period Interrupt Count Cycle Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF, EVF positions

These flag bits indicate alarm interrupts, fixed-period interrupts, time update interrupts, and external event (EVIN) trigger timestamps. When these interrupt events occur, the corresponding flag bits are set to '1'. The flag bits remain '1' until manually cleared to '0', and manual setting of these flag bits to '1' is prohibited.

- AIE, TIE, UIE, EIE bits

These bits are configured to control the interrupt signal output on the INTN pin during alarm interrupts, fixed-period interrupts, time update interrupts, and timestamp events. The default power-up state of these four bits is '0'.

The INTN pin outputs interrupt signals including alarm, fixed-period, time update, and timestamp events. The logic AND operation determines the specific interrupt type through the interrupt flag, which then decides the output signal.

- XST bit

The stop-swing flag is set to '1' when the crystal oscillator stops oscillating, causing the clock circuit to fail in timing. This flag remains '1' until manually cleared to '0', and manual setting to '1' is prohibited. The default power-up state of this flag is '1', indicating inaccurate timing and requiring time configuration. After setting the time, the XST flag can be reset to '0' via IIC, and it will stay '0' until the crystal oscillator stops oscillating again.

- CSEL bit

Sets the time interval for the temperature compensation circuit to start. The default value is '01' (2s) after the chip is powered on.

Table 9-7 Selection of Temperature Compensation Interval

CSEL1	CSEL0	Operation interval
0	0	0.5s
0	1	2s *Default
1	0	10s
1	1	30s

- EN_DET position

The stoppage detection control bit: Setting it to '1' enables the stoppage detection function, while setting it to '0' disables it, saving approximately 50nA of circuit power. The default state of this control bit upon power-up is '1'.

- RESET bit

When RESET is set to '1', the sub-second registers are reset, the clock stops, and the temperature compensation function is disabled.

The reset bit (set to '1') will reset to '0' under three conditions: when IIC termination is detected, a restart condition is triggered, or the IIC bus resets after 0.95 seconds.

9.2.6 Output Precision Adjustment Register (Register 1A)

The 1A register enables fine-tuning of the output frequency for enhanced timing precision. Refer to Table 9-8 for specific adjustment ranges and step values.

Table 9-8 Output Frequency Accuracy Adjustment Table

OFS3	OFS2	OFS1	OFS0	Offset Value (ppm)
0	0	0	0	0.00
0	0	0	1	-0.55
0	0	1	0	-1.10
0	0	1	1	-1.65
0	1	0	0	-2.20
0	1	0	1	-2.75
0	1	1	0	-3.30
0	1	1	1	-3.85
1	0	0	0	4.40
1	0	0	1	3.85
1	0	1	0	3.30
1	0	1	1	2.75
1	1	0	0	2.20
1	1	0	1	1.65
1	1	1	0	1.10
1	1	1	1	0.55

9.2.7 **timestamp-related registers (registers 20-2F)**

Register 20-28 stores the current timestamp with millisecond precision. Registers 29-2F contain timestamp control bits. Registers 30-6F store eight timestamp groups, which can be used as RAM when the timestamp function is disabled.

Table 9-9 Time stamp Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20 ~ 28	Time Stamp	8′ h00	Time Stamp 1/1024s →Year							
29	Stamp Status	8′ h00	EVTP1	EVTP0	○	○	○	○	SXST	○
2A	EVIN Setting	8′ h00	EHL	ET1	ET0	PDN	○	PU	OVW	○
2B	Command Trigger Ctrl	8′ h00	○	○	○	○	○	○	○	COMTG
2C	Command Trigger	8′ h00								
2D	TS Control0	8′ h00	○	○	○	○	○	EISEL	TSCLR	TSRAM
2E	TS Control1	8′ h00	○	○	PRCT1	PRCT0	○	○	○	EXST
2F	TS Control2	8′ h0f	○	○	1′ b1	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0
30 ~ 6F	TS RAM	8′ h00								

*For details on the timestamp feature, see Chapter 11.

10 interrupt capability

10.1 alarm interrupt

Alarm interrupts can occur on specified days, hours, or minutes.

10.1.1 alarm interrupt timing
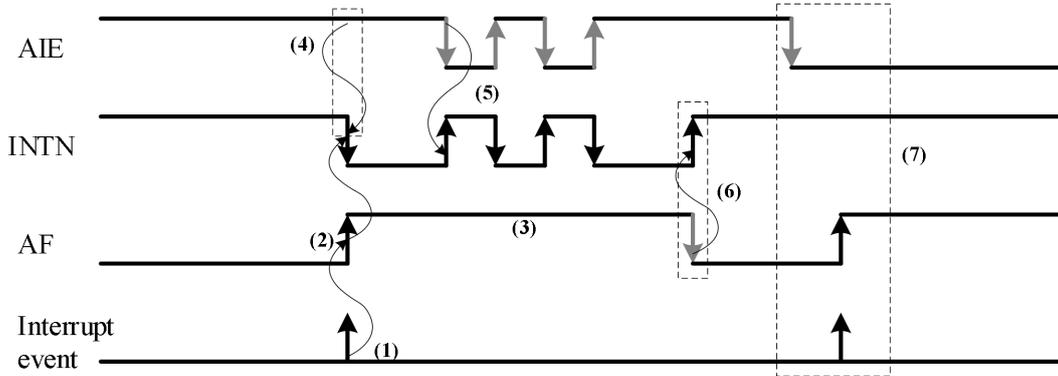
Figure 10-1 Alarm Interrupt Sequence

(1) Set the alarm interrupt to match the hour, minute, date, or day of the week, along with the WADA register. When the set time matches the current time, an alarm interrupt event is triggered.

(2) When an alarm interrupt occurs, the AF flag is set to '1'.

(3) The AF register remains at '1' until manually cleared to '0'.

(4) When an alarm interrupt occurs, INTN outputs low if AIE is '1', and remains high if AIE is '0'.

(5) When INTN = '0', setting AIE to '0' immediately restores INTN to high-impedance state. AIE can control INTN's output state until an alarm interrupt occurs and the AF register is cleared to' 0'.

(6) Clearing the AF register to '0' deactivates the alarm interrupt output, causing INTN to immediately transition from '0' to a high-impedance state.

(7) When an alarm interrupt occurs, if AIE equals '0', INTN remains in a high-impedance state and does not output a low level.

10.1.2 alarm interrupt related register

Table 10-1 Alarm Interrupt Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	8′h00	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	8′h00	**AE**	●	20	10	8	4	2	1
0A	WEEK Alarm	8′h00	**AE**	6	5	4	3	2	1	0
	DAY Alarm			●	20	10	8	4	2	1
0D or 1D	Extension	8′h02	ETS	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8′h01	○	○	UF	TF	**AF**	EVF	○	XST
0F or 1F	Control	8′h42	CSEL1	CSEL0	UIE	TIE	**AIE**	EIE	EN_DET	RESET

- When configuring the alarm interrupt register, it is recommended to set AIE to '0' first to prevent unnecessary hardware interrupts during the operation.

- WADA selects alarm mode: '1' for daily alarm, '0' for weekly alarm.

- An alarm interrupt event sets the AF flag to '1', which remains set until manually reset to '0'.

- When an alarm interrupt occurs, the AIE determines whether to generate an interrupt signal output (if AIE = '1', INTN = '0'; if AIE = '0', INTN = Hi-Z).

- A '0' in the AE bit indicates that the corresponding register must be compared with the clock or calendar register. If the AE bit is '1', the register is not compared, meaning it is always kept synchronized with the clock or calendar register. See the example below:

(1) When register 0A is set to '80', only the minute and hour alarm registers need to be compared with their corresponding clock registers, while the day/month/week register is ignored. Thus, as long as the hour and minute registers match, an alarm interrupt event will occur every day.

(2) Setting the AEs in registers 08,09, and 0A to '1' will trigger an alarm interrupt every minute.

10.2 **fixed periodic interrupt**

The fixed period interrupt can produce alarm events between 244.14μs and 4095min according to a fixed period.

10.2.1 **fixed period interrupt timing**
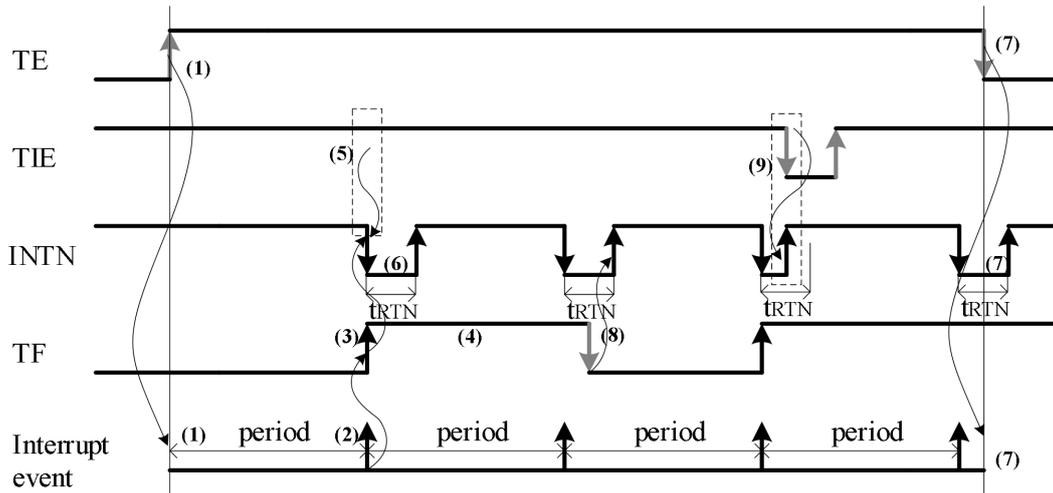
Figure 10-2 Fixed Period Interrupt Timing

(1) When the TE bit is set to '1', the fixed-period counter starts counting down from its preset value.

(2) An interrupt event occurs when the fixed-period counter counts from 001h to 000h. The counter resets to its preset value and continues counting.

(3) When a fixed-period interrupt occurs, the TF register is set to '1'.

(4) The TF register remains at '1' until manually cleared to '0'.

(5) When a fixed-period interrupt event occurs, INTN outputs a low level if TIE is '1', and remains high-impedance if TIE is '0'.

(6) The INTN output remains low for tRTN duration, then automatically reverts to high-impedance state until the next interrupt signal is triggered.

(7) When the TE bit is set to '0', the fixed-period counter stops counting, and INTN outputs high impedance. If the TE bit is set to '0' during INTN = '0', INTN will return to high impedance after the tRTN time.

(8) If TF is cleared to '0' during INTN = '0', it will revert to high-resistance state after INTN persists for tRTN duration.

(9) When TIE is set to '0', INTN immediately returns to high-impedance state. If TIE is reset to '1' during the tRTN period, INTN remains low-level until the tRTN ends.

10.2.2 fixed period interrupt related register

Table 10-2 Fixed Period Interrupt Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	TimerCounter0	8′ h00	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	8′ h00	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	8′ h02	ETS	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8′ h01	○	○	UF	TF	AF	EVF	○	XST
0F or 1F	Control	8′ h42	CSEL1	CSEL0	UIE	TIE	AIE	EIE	EN_DET	RESET

- When configuring fixed-period interrupt registers, it is recommended to first set both TE and TIE to '0' to prevent unnecessary hardware interrupts during operation.

- TSEL1 and TSEL0 are used to set the countdown period for fixed-period interrupts, with the interrupt signal on the INTN pin's reset time automatically synchronized to this countdown period.

Table 10-3 Fixed Cycle Interrupt Counting Period and Automatic Reset Time

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122ms
0	1	64Hz	7.8125ms
1	0	1Hz	7.8125ms
1	1	1/60Hz	7.8125ms

- Register 0B or 1B,0C or 1C sets the default value of the counter (001h to FFFh). The counter counts down to 000h in the TSEL-defined period, triggering a fixed-period interrupt event.

- TE is the enable control bit of the fixed-period counter. When TE is set to '1', the counter starts counting down; when TE is '0', the counter stops counting, terminating the fixed-period interrupt function.

- The occurrence of periodic cycle interrupt events sets the TF flag to '1', which remains set until manually cleared to '0'.

- When a fixed-period interrupt event occurs, TIE determines whether to generate an interrupt signal output (if TIE = '1', INTN = '0'; if TIE = '0', INTN = Hi-Z).

Table 10-4 Example of Fixed Period Interrupt Period

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
......	......	......	......	......
2048	500ms	32s	2048s	2048min
......	......	......	......	......
4095	0.9998s	63.984s	4095s	4095min

10.3 Time update interruption

Based on the set value, the time update interrupt generates alarm events at second or minute intervals.
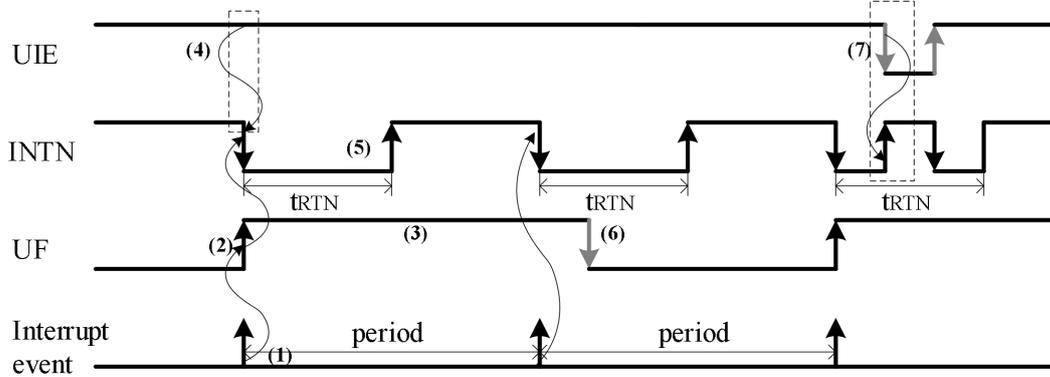
10.3.1 interrupt timing of time update

Figure 10-3 Time Update Interrupt Sequence

(1) The USEL register determines whether the chip is in second or minute update interrupt mode. When the corresponding second or minute register updates, a time update interrupt event is generated.

(2) When the time update interrupt occurs, the UF register is set to '1'.

(3) The UF register will remain at '1' until manually cleared to '0'.

(4) When a time update interrupt event occurs, if UIE = '1', INTN outputs a low level; if UIE = '0', INTN remains in a high-impedance state.

(5) The INTN output remains low for tRTN duration, then automatically reverts to high-impedance state until the next interrupt signal is triggered.

(6) If the UF is cleared to '0' during the INTN = '0' period, INTN will revert to high-impedance state after the tRTN time.

(7) If the UIE is set to '0' during the INTN = '0' period, INTN immediately returns to the high-impedance state, terminating the interrupt signal output. If the UIE is reset to '1' again during the tRTN period, INTN reverts to the low-level state until the end of tRTN.

10.3.2 time update interrupt register

Table 10-5 Time Update Interrupt Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	8′h02	ETS	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8′h01	○	○	UF	TF	AF	EVF	○	XST
0F or 1F	Control	8′h42	CSEL1	CSEL0	UIE	TIE	AIE	EIE	EN_DET	RESET

- When configuring the timer interrupt register, set the UIE to '0' first to prevent unnecessary hardware interrupts during operation.

- The USEL signal is used to set the interrupt mode to second or minute updates.

Table 10-6 Time Update Interrupt Mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event sets the UF flag to '1', which remains set until manually cleared to '0'.

- When a time update interrupt event occurs, the UIE determines whether to generate an interrupt signal output (if UIE = '1', INTN = '0'; if UIE = '0', INTN = Hi-Z).

11 Timestamp feature

The JXR271T-GA features timestamp functionality, configurable to trigger via external events, internal events, or IIC commands, with continuous storage capacity for up to 8 timestamp groups.

11.1 functional description

The timestamp function of the JXR271T-GA chip can be activated through the following three methods:

• External event trigger (via EVIN Pin)

• Internal event trigger (crystal oscillator stoppage)

• IIC instruction trigger (via IIC operation on the 2C register)

• When a timestamp event is triggered, the current timestamp is stored in registers 20 to 28, and can be configured to sequentially store the timestamp information into RAM addresses 30 to 6F.

11.2 general control

The timestamp information is stored in the corresponding register and RAM in the form of Table 10-1.

Table 11-1 Timestamp Information Storage Format

Address		Function
20		1/1024s
21	30, 38, 40, 48, 50, 58, 60, 68	1/512s
22	31, 39, 41, 49, 51, 59, 61, 69	SEC
23	32, 3A, 42, 4A, 52, 5A, 62, 6A	MIN
24	33, 3B, 43, 4B, 53, 5B, 63, 6B	HOUR
25		WEEK
26	34, 3C, 44, 4C, 54, 5C, 64, 6C	DAY
27	35, 3D, 45, 4D, 55, 5D, 65, 6D	MONTH
28	36, 3E, 46, 4E, 56, 5E, 66, 6E	YEAR
29	37, 3F, 47, 4F, 57, 5F, 67, 6F	Stamp Status

Users can configure PRCT1 and PRCT0 to prevent repeated timestamp triggering after a set interval. This avoids redundant timestamp generation due to external noise interference during the same event, which could otherwise consume system resources.

Table 11-2 Timestamp Mask Settings

PRCT1	PRCT0	Decription
0	0	Do not control timestamp triggers
0	1	No new timestamp will be triggered within 1 second
1	0	No new timestamps will be triggered within 1 minute
1	1	No new timestamps will be triggered within 5 minutes

When a timestamp trigger occurs, it not only stores the time information but also synchronizes the trigger type information in both EVTP1 and EVTP0, enabling easy identification of the specific cause behind the trigger.

Table 11-3 Timestamp Event Type Indicator

EVTP1	EVTP0	Decription
0	0	No timestamp triggered
0	1	External Event Trigger Timestamp
1	0	IIC trigger timestamp
1	1	Internal event (lockout) trigger timestamp

11.3 External Event Trigger Timestamp

Table 11-4 External Event Trigger Timestamp Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	8′h02	**ETS**	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8′h01	○	○	UF	TF	AF	**EVF**	○	XST
0F or 1F	Control	8′h42	CSEL1	CSEL0	UIE	TIE	AIE	**EIE**	EN_DET	RESET
2A	EVIN Setting	8′h00	**EHL**	**ET1**	**ET0**	**PDN**	○	**PU**	OVW	○

- ETS site

The timestamp function is enabled by external event trigger. When ETS is set to '1', external events can trigger the timestamp via the EVIN pin. When ETS is set to '0', the EVIN pin does not trigger the timestamp function.

- EVF position

The timestamp flag is triggered by external events. When an external event activates the timestamp via EVIN, the EVF bit is automatically set to '1' and remains set until manually cleared to '0'. This flag cannot be set to '1'.

- EIE bit

Hardware interrupt enable control: When EIE is set to '1', the INTN pin outputs a low level after the timestamp is triggered. When EIE is set to '0', the timestamp triggers only a software response without interrupt information output through the INTN pin.

- EHL, PDN, PU position

The EHL controls external events by triggering timestamps via EVIN, requiring coordination with PDN and PU. Refer to Table 10-5 for detailed control methods.

Table 11-5 External Event Trigger Time Stamp Control

PDN	PU	EHL	Description
0	0	0	The EVIN Pin requires an external pull-up resistor and a low-pulse trigger timestamp.
		1	The EVIN Pin requires an external pull-down resistor and a high-pulse trigger timestamp.
0	1	0	The EVIN Pin features an integrated pull-up resistor and low-pulse-trigger timestamp
		1	Unauthorized configuration
1	0	0	Unauthorized configuration
		1	The EVIN Pin features a built-in pull-down resistor and high-pulse-trigger timestamp
1	1	0	The EVIN Pin requires an external pull-up resistor and a low-pulse trigger timestamp.
		1	The EVIN Pin requires an external pull-down resistor and a high-pulse trigger timestamp.

- ET1, ET0 bits

To prevent EVIN pin burrs from accidentally triggering timestamps, configure the filter function to remove unnecessary interference. EVIN pulses below the set filter threshold will not trigger timestamps.

Table 11-6 EVIN Filter Settings

ET1	ET0	Description
0	0	Do not set pulse width filter
0	1	EVIN pulses with a pulse width less than 3.9ms will not trigger timestamps.
1	0	EVIN pulses with a pulse width less than 15.6ms will not trigger timestamps.
1	1	EVIN pulses with a pulse width less than 125ms will not trigger timestamps.

11.4 **IIC trigger timestamp**

Table 11-7 IIC Trigger Timestamp Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2B	Command Trigger Ctrl	8′ h00	○	○	○	○	○	○	○	COMTG
2C	Command Trigger	8′ h00								

- COMTG bit

The IIC event trigger timestamp control is enabled. When COMTG is set to '1', the IIC event trigger timestamp function is enabled; when COMTG is set to '0', the function is disabled.

When the IIC event trigger timestamp function is enabled, the timestamp can be activated by sending a read 2C register command via the IIC bus.

11.5 **Internal event (lockout) trigger timestamp**

Table 11-8 Internal Event Timestamp Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29	Stamp Status	8′ h00	EVTP1	EVTP0	○	○	○	○	**SXST**	○
2E	TS Control1	8′ h00	○	○	PRCT1	PRCT0	○	○	○	**EXST**

- EXST bit

Enable the internal event trigger timestamp control. Set EXST to '1' to enable the internal event trigger timestamp function, and set EXST to '0' to disable it.

- SXST bit

The timestamp type flag indicates that the current timestamp is triggered by an internal event when both EVTP1 and EVTP0 are set to '1'. By setting the SCST flag to '1', the system confirms the occurrence of a stoppage.

11.6 **time stamp RAM**

Table 11-9 Timestamp RAM-related registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	EVIN Setting	8′ h00	EHL	ET1	ET0	PDN	○	PU	**OVW**	○
2D	TS Control0	8′ h00	○	○	○	○	○	**EISEL**	**TSCLR**	**TSRAM**
2F	TS Control2	8′ h0f	○	○	1′ b1	**TSFUL**	**TSEMP**	**TSAD2**	**TSAD1**	**TSAD0**

- OVW bit

The RAM address pointer operates in a cyclic mode. When the Overwrite (OVW) setting is '1', timestamps stored in RAM are overwritten on a first-in-first-out basis. When OVW is '0', timestamps are not overwritten and new ones are discarded upon full storage.

Table 11-10 Timestamp RAM Cycle Control

OVW	Description
0	The RAM address pointer does not loop (000 (001 (... (111 (stop))
1	RAM address pointer loop (000 (001 (... (111 (000 (...))

- EISEL site

The hardware interrupt output mode control bit operates as follows: When EISEL is set to '1', it activates the RAM FULL mode, triggering a hardware interrupt upon detecting full RAM for timestamps. When EISEL is set to '0', the system operates in normal interrupt mode, where timestamps can directly trigger hardware interrupts (note that hardware interrupt generation also depends on the EIE status).

- TSCLR bit

This function initializes the RAM address pointer. When the TSCLR bit is set to '1', the TSFUL bit is initialized to '0', while the TSEMP and TSAD bits are set to '1'.

- TSRAM bit

The RAM mode selection bit determines the timestamp storage location: When TSRAM is set to '1', timestamp data is simultaneously stored in registers 20-29 and 30-6F; when TSRAM is set to '0', the data is stored exclusively in registers 20-29.

- TSFL position

The RAM full indicator bit is set to '1' when the RAM area is full and the TSRAM reads the value as '1'.

- TSEMP bit

The RAM area status bit indicates that the TSEMP reads '1' when no timestamp information is stored in the RAM area.

- TSAD2, TSAD1, TSAD0

Table 11-11 RAM refers to the corresponding relationship

TSAD2	TSAD1	TSAD0	Address
0	0	0	30 ~ 37
0	0	1	38 ~ 3F
0	1	0	40 ~ 47
0	1	1	48 ~ 4F
1	0	0	50 ~ 57
1	0	1	58 ~ 5F
1	1	0	60 ~ 67
1	1	1	68 ~ 6F, Default

12 IIC BI

12.1 Characteristics of IIC Bus

The IIC is a bidirectional communication interface where the signal line (SDA) and clock line (SCL) must be connected to VDD via pull-up resistors. The IIC bus port must be configured as an open-drain structure to enable multi-device wiring and connection.

12.2 data transmission

Each SCL clock cycle transmits 1bit of data. During transmission, data on the SDA line changes when the SCL is at low level; during reception, stable and valid data can be obtained from the SDA line when the SCL is at high level.

12.3 Initial and terminal conditions

In idle state, both SCL and SDA remain at high level. During the high-level state of SCL, the falling edge of SDA serves as the trigger for IIC communication, while the rising edge of SDA acts as the termination signal for IIC communication.
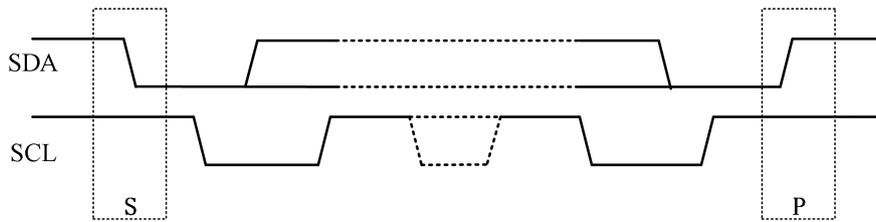
Figure 12-1 Initial and termination conditions of IIC

12.4 Select device (from address)

The IIC bus lacks a chip select signal. The master device selects a slave device by sending a unique fixed device number (slave address), and the selected slave device responds to establish communication with the master.

The address consists of 7 bits of data, with 4 bits (Group 1) and 3 bits (Group 2). The slave address for the JXR271T-GA is "0110010". During communication, the slave address and R/W selection bit are transmitted as 8-bit data.

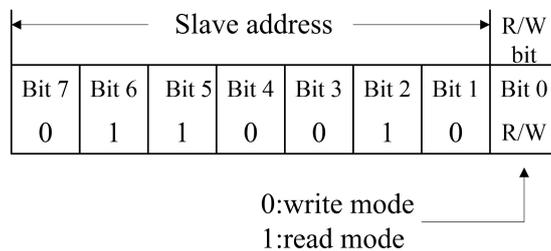| Slave address							R/W bit
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	1	0	R/W

0:write mode
1:read mode

Figure 12-2 IIC Address Schematic

12.5 system configuration

The device that controls the data transmission is called the master device, the device controlled by the master device is called the slave device, the device that sends the data is called the sender,

the device that receives the data is called the receiver.

In the JXR271T-GA system, the CPU or other control devices act as master devices, while the JXR271T-GA chip itself serves as a slave device. Both master and slave devices can function as either the transmitter or the receiver.
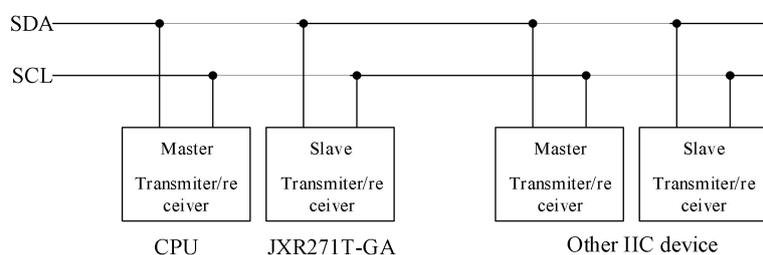

Figure 12-3 IIC System Configuration

12.6 Acknowledge signal

The IIC bus imposes no restrictions on the number of bytes transmitted between start and stop conditions. Upon completion of each byte transfer, the transmitter must release the SDA bus and provide one SCL clock to receive the acknowledge signal. If the receiver successfully receives 8-bit data, it must set the SDA to '0' after the clock cycle of the final 1-bit data transmission. The transmitter then interprets this low level as the successful acknowledge signal. One clock cycle later, the receiver releases the SDA bus and prepares to receive new data.

The IIC bus terminates data transmission when the following conditions are met:

(1) When the master device acts as the transmitter, it terminates the transmission upon receiving the acknowledge signal from the slave device.

(2) When the main device acts as the receiver, it sends a '1' as the acknowledge signal after successfully receiving 8-bit data, followed by the termination condition.

12.7 **IIC bus control**

This section describes the IIC bus communication timing when the CPU is the master device and the JXR271T-GA is the slave device.

12.7.1 **addressed write operation**

The JXR271T-GA features an auto-increment address system. Once the target address is set, it only requires continuous data transmission, with the address bit incrementing automatically.
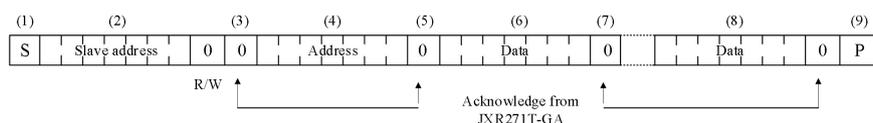

Figure 12-4 specifies the address write operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR271T-GA slave address and sets the R/W bit to write mode.

(3) JXR271T-GA sends the acknowledge signal.

(4) The CPU sends the write register address to JXR271T-GA.

(5) JXR271T-GA sends the acknowledge signal.

(6) The CPU sends data to the register at the address specified in (4).

(7) JXR271T-GA sends the acknowledge signal.

(8) Repeat steps (6) and (7), where the address of the write register in JXR271T-GA will increment automatically.

(9) The CPU sends the Stop bit [P].

12.7.2 **addressed read operation**

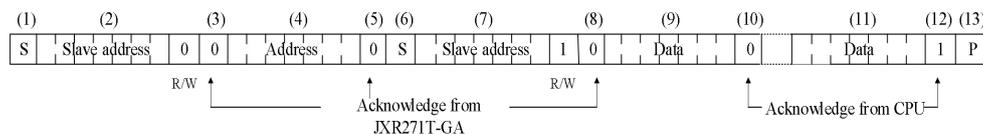After writing to the register, the CPU can read the register data by setting the read mode.

Figure 12-5 Specified Address Read Operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR271T-GA slave address and sets the R/W bit to write mode.

(3) JXR271T-GA sends the acknowledge signal.

(4) The CPU sends the read register address to JXR271T-GA.

(5) JXR271T-GA sends the acknowledge signal.

(6) The CPU sends the restart bit.

(7) The CPU sends the JXR271T-GA slave address and sets it to read mode through the read/write bit.

(8) The JXR271T-GA sends the acknowledge signal, then the CPU acting as the receiver and the JXR271T-GA as the transmitter.

(9) The data in the register at the specified address in JXR271T-GA Send (4).

(10) The CPU sends the acknowledge signal to JXR271T-GA.

(11) Repeat steps (9) and (10), where the address of the read register in JXR271T-GA will increment automatically.

(12) The CPU sends No acknowledge signal to JXR271T-GA.

(13) The CPU sends the stop bit [P].

12.7.3 Unspecified address read operation

The master device can directly enter read mode to access the register contents of the slave device. As the master device does not specify the read operation address, the slave device starts reading from the address one unit higher than the previous IIC operation address.
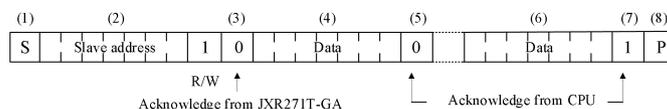

Figure 12-6 Unspecified address read operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR271T-GA slave address and sets it to read mode through the read/write bit.

(3) The JXR271T-GA sends the acknowledge signal, then the CPU acting as the receiver and the JXR271T-GA as the transmitter.

(4) The JXR271T-GA automatically increments the register address and transmits the register data.

(5) The CPU sends the acknowledge signal to JXR271T-GA.

(6) When repeating steps (4) and (5), the address of the read register in JXR271T-GA will increment automatically.

(7) The CPU sends the No acknowledge signal to JXR271T-GA.

(8) The CPU sends the stop bit [P].

Appendix

direction for use

1. The product features an electrostatic protection rating of HBM ±2.0kV and CDM ±2.0kV. During operation, precautions must be taken to prevent electrostatic discharge.

2. During operation, power spikes exceeding 8.25V may trigger latch-up effects and circuit damage. To ensure stable chip operation, install a decoupling capacitor (minimum 0.1uF) near the clock chip's power pin.

3. Because the clock chip is a low power integrated circuit, it is necessary to avoid placing any high noise components around the clock chip.

4. Leaving the chip's input pins floating may increase current power consumption. During operation, these pins should be connected to a fixed potential (VDD or VSS).

5. The chip's humidity sensitivity rating is Level 2. From unpacking to board soldering, the workshop storage environment must maintain temperature and humidity below 30°C and 60%RH respectively, with a maximum storage duration of one year.

6. During reflow soldering, the peak temperature must be strictly controlled to not exceed 260°C, with a maximum of two reflow cycles allowed. Manual soldering should not exceed 350°C, and the soldering duration should not exceed 5 seconds. Exceeding these limits may damage the built-in crystal oscillator, causing excessive clock deviation or even complete stoppage. Refer to the reflow curve diagram below for guidance.

| Profiles Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts Min) Temperature Max (Ts Max) Time (Ts) from (Ts Min to Ts Max)	 150℃ 200℃ 60～120 seconds
Ramp-up rate (TL to TP)	3℃/second Max
Liquidous Temperature (TL) Time (TL) maintained above TL	217℃ 35 seconds Max
Peak/Classification Temperature (TP)	245±5℃
Time within 5℃ of actual Peak Temperature (TP)	5 seconds Max
Ramp-down rate (TP to TL)	6℃/second Max
Time 25℃ to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max

Encapsulation size

TOP VIEW

SIDE VIEW

BOTTOM VIEW
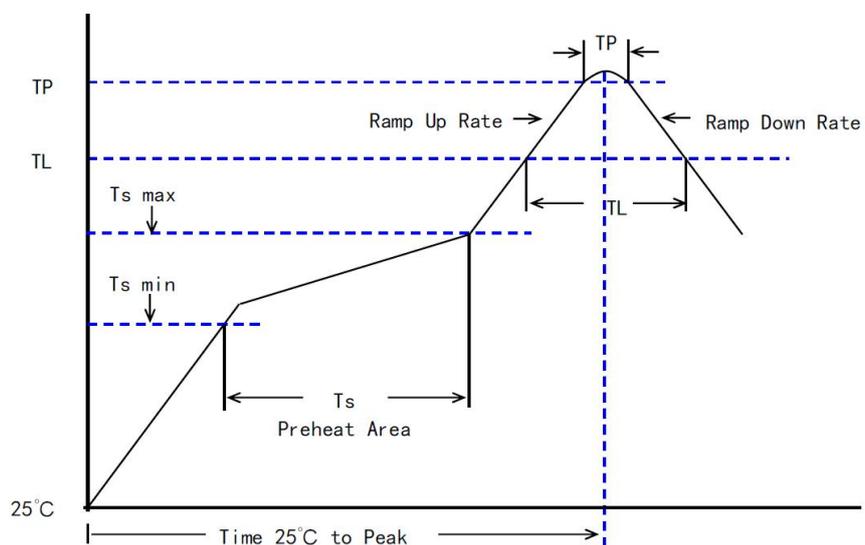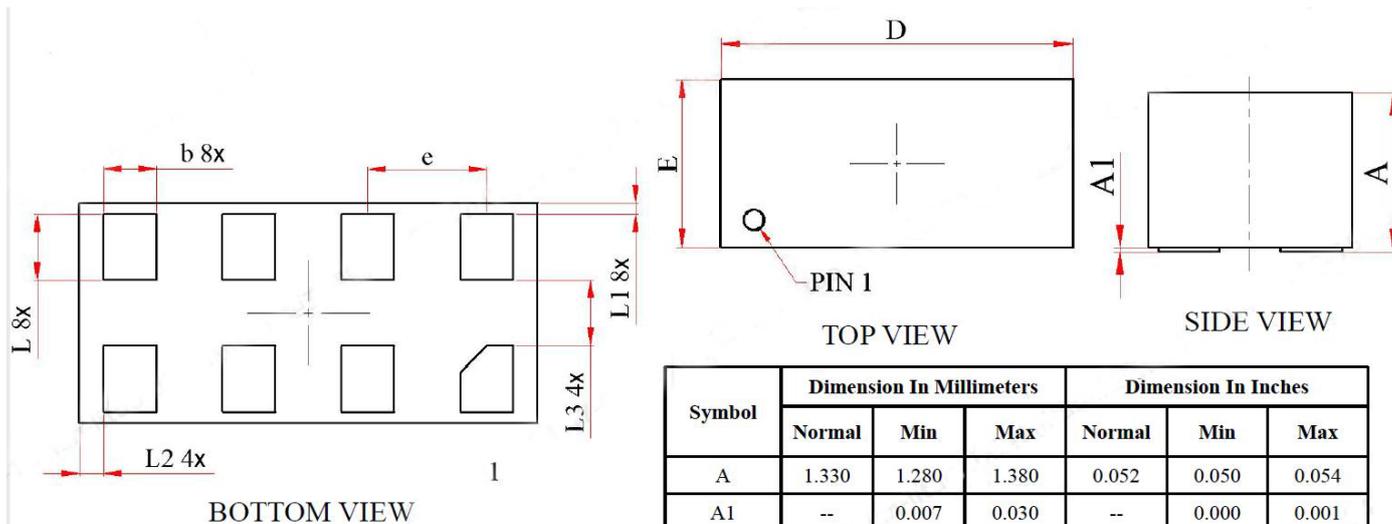
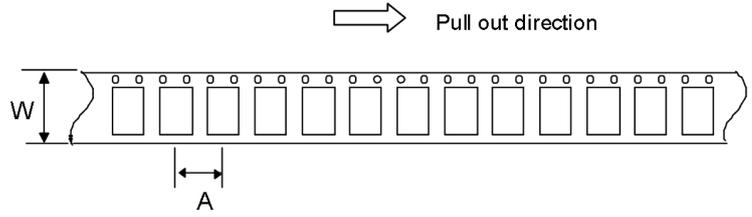| Symbol	Dimension In Millimeters			Dimension In Inches		
	Normal	Min	Max	Normal	Min	Max
A	1.330	1.280	1.380	0.052	0.050	0.054
A1	--	0.007	0.030	--	0.000	0.001
D	3.470	3.440	3.500	0.137	0.136	0.138
E	1.720	1.690	1.750	0.068	0.067	0.069
b	0.400	0.350	0.450	0.016	0.014	0.018
L	0.500	0.450	0.550	0.020	0.018	0.022
L1	0.110	0.085	0.135	0.004	0.003	0.005
L2	0.185	0.160	0.210	0.007	0.006	0.008
L3	0.500 REF			0.020 REF		
e	0.900 BSC			0.035 BSC		

Unit: mm

Recommended pad size
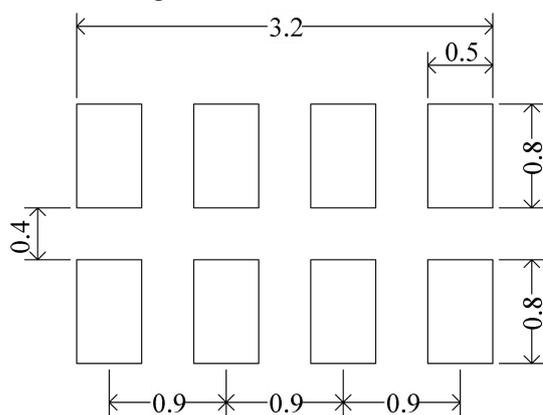
packing specifications

Emboss Taping (TL)

Symbol	DFN8
A	4
W	12

Unit : mm

Symbol	DFN8
A	330
W	12

Unit : mm

Pull out direction

End of taping

Empty area	Occupancy area 4000 units per reel	Empty area

Area of seal by covertape

Beginning of taping

TL

Bar-code label

Put in the outer box

Static shield bag
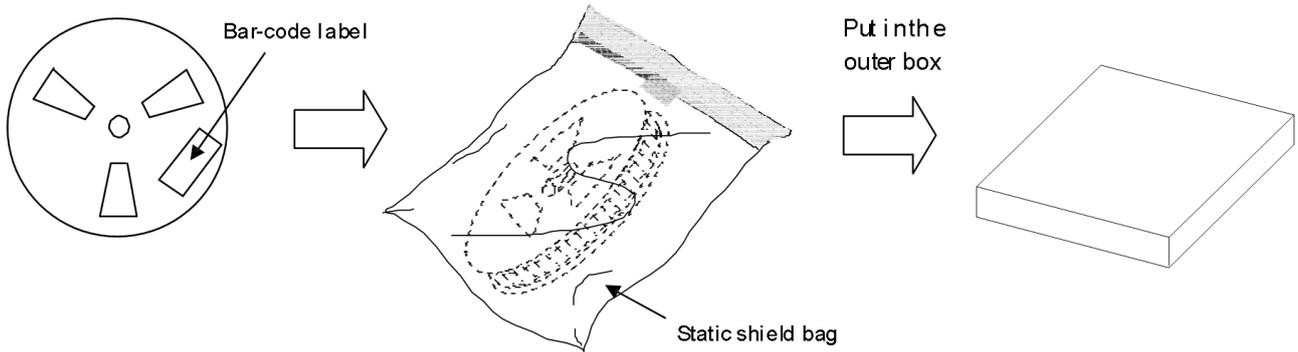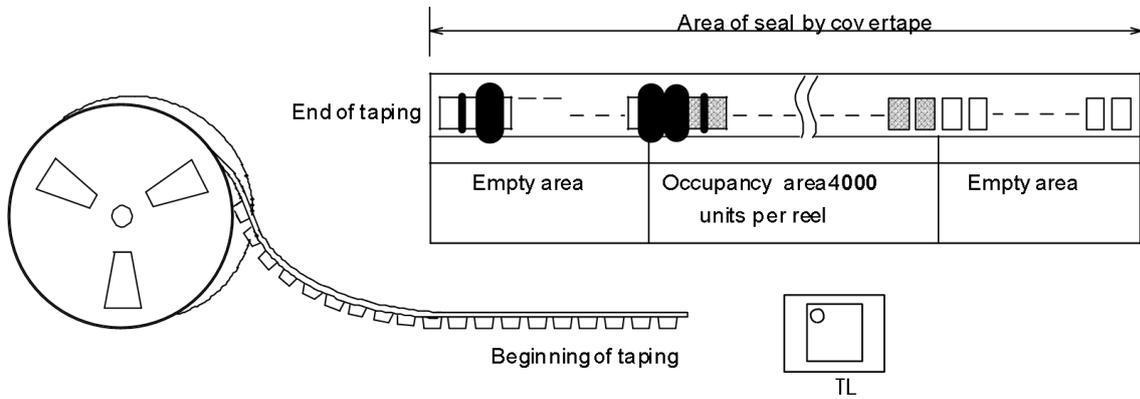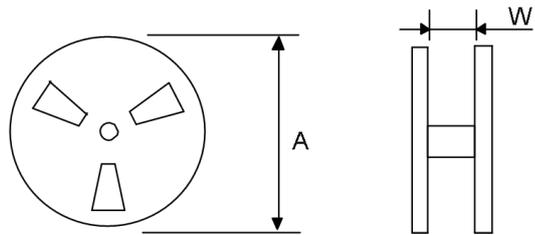
Order Information

product name	material number	encapsulation form	Packaging format	Minimum order quantity
JXR271T-GA(UA)	OSC0B271TGA01000	DFN8	13-inch reel	4000
JXR271T-GA(UB)	OSC0B271TGA02000	DFN8	13-inch reel	4000

Product Label Description