JXR131 User Manual

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Content

1. Overview

JXR131 is a high accuracy, real-time clock module with IIC interface; The minimum timing unit is second, can realize automatic leap year correction, and can provide alarm function, fixed-cycle Timer Interrupt function, time update interrupt function and 32.768KHz/1024Hz/1Hz clock output function.

The chip has the the battery backup switchover function, after the main power domain powering down, the standby power supply will be automatically switched to supply power for the chip.

2. Characteristics

- Supports IIC-Bus's high-speed mode (Up to 400 kHz)
- Multiple interrupt functions: timer alarm interrupt, fixed-cycle Timer Interrupt， time update interrupt
- 32.768KHz/1024Hz/1Hz clock output with enable control
- Support full calendar function from 2000 to 2099, support leap year automatic correction
- Automatic power switch and can provide trickle charging for spare batteries
- 32.768kHz/1024Hz/32Hz/1Hz output
- Wide interface voltage range: 1.6V ~ 5.5V
- Wide time-keeping voltage range: 1.1V ~ 5.5V
- Low current power consumption: 0.7μA@3V(Typ)

3. Block Diagram

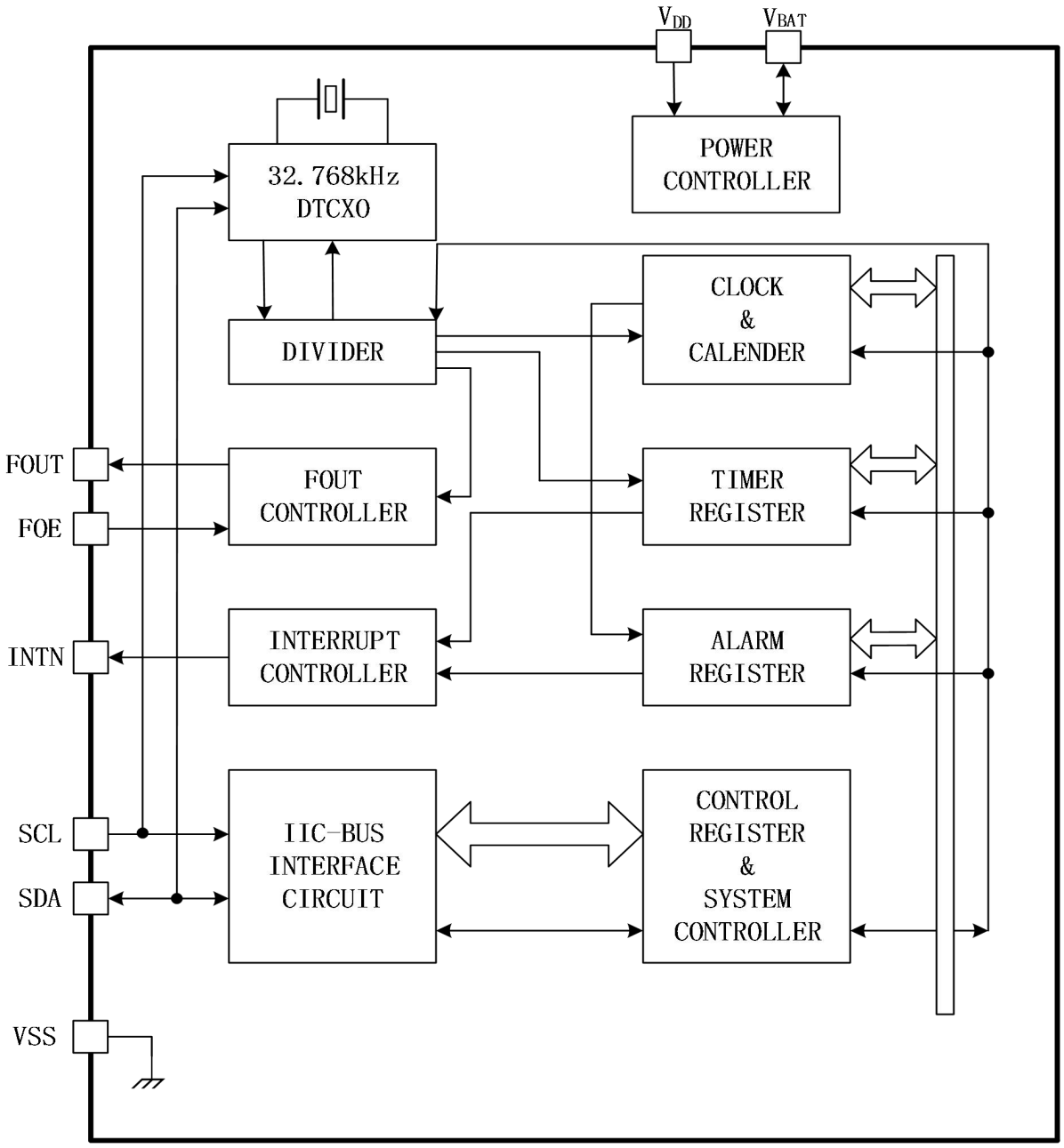


Figure 3- 1 JXR131 system block diagram

4. Terminal description

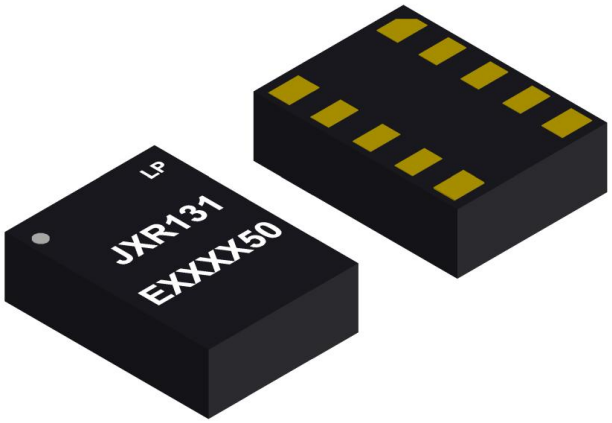


Figure 4- 1 JXR131 package form

Figure 4- 2 JXR131 Pin Description

Pin name	I/O	Function
1. NC	---	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.
2. SCL	IN	This is the serial clock input pin for IIC Bus communications.
3. SDA	INOUT	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for IIC communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
4. FOUT	OUTPUT	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
5.FOE	IN	This is the serial clock input pin for IIC Bus communications.
6. INTN	OUTPUT	the output port of the Interrupt , N-ch open the leakage output
7. VSS	GROUND	Power grounding terminal
8. VDD	POWER	This pin is connected to a positive power supply.
9. NC	---	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.
10. VBAT	POWER	This is the power supply pin for backup battery. Connect this pin to a large-capacity capacitor, a secondary battery or similar. When the battery switchover function is not needed, VBAT must be connected to VDD.

5. Absolute Maximum ratings

Table 5- 1 Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply voltage*1	V_{DD}	Voltage between V_{DD} and V_{SS}	-0.5 to 6.5	V
Input voltage*1, *2	V_{IN}	FOE, SCL, SDA pins	-0.5 to V_{DD}+0.5	V
Output voltage*1, *2	V_{OUT}	FOUT, SDA, INTN pins	-0.5 to V_{DD}+0.5	V
Storage temperature	T_{STG}	Store separately, unpacked	-55 to 125	℃

*1:Each electrical indicator shall not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of relevant parameters, reliability reduction and even chip failure.

*2:This V_{DD} refers to the range of V_{DD} under recommended operating conditions.

6. Recommended operating conditions

Table 6- 1 Recommend Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Interface voltage	1.5	3.0	5.5	V
Clock supply voltage	V_{CLK}	operating voltage of Oscillator module	2.2	3.0	5.5	V
Operating temperature range	T_{OPR}	---	-40	25	125	℃

* Any operation beyond the recommended range in the above table can greatly affect the reliability of the chip.

7. Frequency characteristics

Table 7- 1 Frequency Characteristics

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Frequency Stability	Δf/f	Ta=25℃, V_{DD}=3.0V		5±23		$\times10^{-6}$
Frequency/voltage characteristics	Δf/f/V	Ta=25℃，V_{DD}=1.1V~5.5V	-2.0		+2.0	$\times10^{-6}$/V
Oscillation start time	T_{STA}	Ta=25℃, V_{DD}=1.8V			1.0	S
		Ta=-40℃~85℃, V_{DD}=1.8V~5.5V			2.0	
Aging	fa	Ta=25 ℃, V_{DD}=3.0V, first year	-5.0		+5.0	$\times10^{-6}$/year

8. Electrical characteristics

8.1 DC Characteristics

Table 8- 1 DC Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{DD1}	FOE = GND FOUT = '0'	V_{DD} = 5.0 V		1.2	3.0	µA
	I_{DD2}		V_{DD} = 3.0 V		0.7	2.0	
	I_{DD3}	FOE = V_{DD} FOUT = 32.768kHz CL = 0pF	V_{DD} = 5.0 V		3.6		nA
	I_{DD4}		V_{DD} = 3.0 V		2.9		
	I_{DD5}	FOE = V_{DD} FOUT = 32.768kHz CL = 30pF	V_{DD} = 5.0 V		7.5		V
	I_{DD6}		V_{DD} = 3.0 V		6.2		V
High-level input voltage	VIH	FOE, SCL, SDA, pins	VDD = 2.2V ~ 5.5V	0.7*VDD		VDD+0.3	V
Low-level input voltage	VIL	FOE, SCL, SDA pins	VDD = 2.2V ~ 5.5V	- 0.3		0.3*VDD	V
High-level output voltage	VOH	FOUT pin	IOH = -1mA	VDD - 0.3		VDD	V
Low-level output voltage	VOL	FOUT, INTN pins	IOL = 1mA	GND		GND+0.3	V
		SDA pin	VDD ≥ 2V IOL = 3mA	GND		GND+0.3	V
Input leakage current	I_{LK}	FOE, SCL, SDA, V_{IN}=VDD or GND		-0.1		0.1	µA
Output leakage current	I_{OZ}	INTN, FOUT, SDA, VIN=VDD or GND		-0.1		0.1	µA

8.2 AC Characteristics

Table 8-2 AC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	---			400	KHz
Start condition setup time	$t_{SU;STA}$	---	0.6			μS
Start condition hold time	$t_{HD;STA}$	---	0.6			μS
Data setup time	$t_{SU;DAT}$	---	100			nS
Data hold time	$t_{HD;DAT}$	---	0		700	nS
Stop condition setup time	$t_{SU;STO}$	---	0.6			μS
Bus idle time	t_{BUF}	Between start condition and stop condition	1.3			μS
Time when SCL = "L"	t_{LOW}	---	1.3			μS
Time when SCL = "H"	t_{HIGH}	---	0.6			μS
Rise time for SCL and SDA	t_r	---			0.3	μS
Fall time for SCL and SDA	t_f	---			0.3	μS
Allowable spike time on bus	t_{SP}	---			50	nS

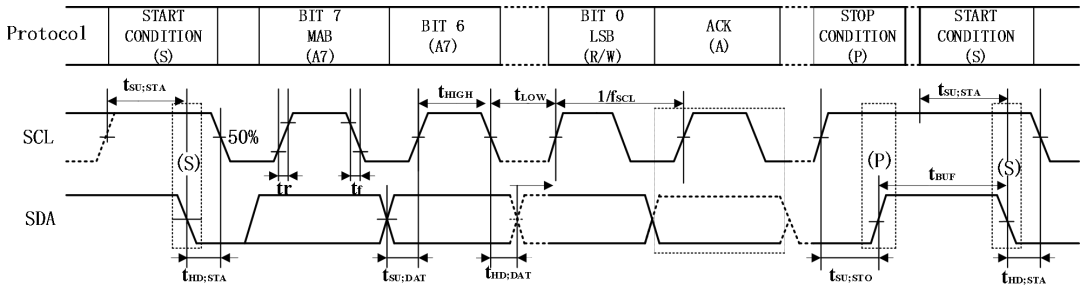


Figure 8- 1 IIC timing legend

* The IIC data transfer is located between the start condition and the end condition, and the data transfer operation must be completed within 0.95S time, after which the IIC bus will be reset by the internal time.

9 Registers

9.1 Register summary table

Table 9- 1 Register Table

Address[h]	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70	MSEC[9:8]	○	○	○	○	○	○	512	256
71	MSEC[7:0]	128	64	32	16	8	4	2	1
00 or 10	SEC	○	40	20	10	8	4	2	1
01 or 11	MIN	○	40	20	10	8	4	2	1
02 or 12	HOUR	○	○	20	10	8	4	2	1
03 or 13	WEEK	○	6	5	4	3	2	1	0
04 or 14	DAY	○	○	20	10	8	4	2	1
05 or 15	MONTH	○	○	○	10	8	4	2	1
06 or 16	YEAR	80	40	20	10	8	4	2	1
07	RAM	•	•	•	•	•	•	•	•
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0B or 1B	TimerCounter0	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	○	○	XST
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET
19	PW Control	CHGEN	INIEN	○	○	○	SWSEL	SMPT1	SMPT0
1A	Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0

Address[h]	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20 | 23	RAM	User Register 32 bits（4*8 bits）							

* Make sure to write a legal value to the calendar clock register, otherwise the chip will not be able to perform the correct timing operation.

*Register bits marked with ○ are read-only bits and read values are "0"; Register bits marked can be used as RAM to perform reading and writing operations.

*If the alarm interrupt function is not set (AIE= "0"), registers 08~0A can be used as RAM.

*If the fixed period interrupt function (TE=TIE= "0") is not set, registers 0B, 0C can be used as RAM.

*UF, TF, AF bits are only allowed to be written to "0".

*When the chip is powered on, the VLF bits are preset to "1", FSEL1, FSEL0, UIE, TIE, AIE bits are preset to "0".

9.2 Details of Registers

9.2.1 Time and date registers（Reg 00~06 or 10~16）

- **Data form**

With the exception of the week register (register 03 or 13), the data is in BCD code form. For example, the value "0101 1001" in the second register means that it is currently 59 seconds.

The timing mode is fixed to the 24-hour system.

- **Year register and leap year**

The year register ranges from 00 to 99, and then returns to 00 after 99; The year is a leap year when the value represented by the register is divisible by 4. The calendar is valid from 2000 to 2099.

- **Week Register**

The week register has a total of 7 significant bits (bit0~bit2）， showed on table 10-2.

table 9- 2 Week register table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	week
0	0	0	0	0	0	1	日
0	0	0	0	0	1	0	一
0	0	0	0	1	0	0	二
0	0	0	1	0	0	0	三
0	0	1	0	0	0	0	四
0	1	0	0	0	0	0	五
1	0	0	0	0	0	0	六

9.2.2 Millisecond registers（Reg 70、71）

These register are read-only registers, not supported been wrote. They are mainly used for timing milliseconds, which can provide more precise clocking. These registers hold 10 effective bits totally.(top 2 bits in 70 register, and lower 8 bits in 71 register),.

Reg 70 and 71 will be set to 0 and restart timing just after configuring the second register,.

9.2.3 Alarm register（Reg 08~0A）

The alarm can be set to X hours X minutes on X days of the week or X hours X minutes on X days of the month (week alarm mode and day alarm mode), and the alarm mode can be set via the WADA bit of register 0D or 1D.

Each Alarm register has AE (Alarm Enable) bits (bit7). When the AE bit of an alarm register is "0", the set value of the register needs to be compared with the corresponding timer register. When the value is consistent, the output alarm is interrupted; If the AE bit is "1", the corresponding alarm register value is ignored, that is, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is consistent with the corresponding timing register value.

When the WEEK ALARM mode is selected, several days of the week can be selected at the same time, that is, the week alarm function bit0 to bit6 in register 0A can have several bits of "1" at the same time. Refer to Table 9-3 for the corresponding relationship in week alarm mode.

Table 9- 3 Week alarm mode register 0A table

Register	Function	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0A	Week alarm	Sat	Fri	Thu	Wed	Tue	Mon	Sun

9.2.4 Fixed cycle counter control register (register 0B or 1B, 0C or 1C)

These two registers are used to set the preset backcount value of the fixed period interrupt. When the value in the above two registers changes from 001h to 000h, the fixed period interrupt event occurs, TF is set to "1" and INTN outputs a low level (if TIE is "1"); The 0B or 1B, 0C or 1C registers are then reset to the preset value and the countdown process is restarted.

9.2.5 Control register and Flag register (registers 0D~0F or 1D~1F)

- WADA bit

Alarm Interrupt mode selection bit, when set to "1", for daily alarm mode, when set to "0", for weekly alarm mode.

- USEL bit

The period used to set the time update interrupt; The bit is an indefinite value when the chip is powered on, and needs to be manually configured during use.

Time Update Interrupt mode selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

When the position is "1", the counter with fixed period interruption starts to count backwards, and when it is set to "0", it stops counting backwards.

- FSEL bit

Set the output frequency of the FOUT port. For details, see Table 9-5. After the chip is powered on, the default value is 00.

FOUT output frequency selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768kHz * Default
0	1	1024Hz
1	0	1Hz
1	1	32.768kHz

- TSEL bit

The counting period used to set the fixed period interrupt.

Fixed cycle interrupt count cycle selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF bit

They are alarm interrupt, fixed period interrupt, time update interrupt flag bits; When the above interrupt event occurs, the corresponding flag bit is set to "1". The flag bit will remain as "1" until it is cleared to "0" manually. Do not manually set the flag position to "1".

- AIE, TIE, UIE bit

They are used to set the interrupt signal output on the INTN pin when alarm interrupt, fixed period interrupt, time update interrupt event occurs; The power-on default value of the three bits is "0".

The interrupt signal output on the INTN pin is alarm interrupt, fixed period interrupt, time update interrupt logic or, through the interrupt flag bit to judge the specific interrupt situation and determine the interrupt signal output.

- VLF bit

Low voltage detection flag bit; This bit is set to "1" when the power supply voltage is detected to drop below

1.8V, causing the clock circuit to not work properly, or when the power-on reset signal is detected. This flag bit will remain as "1" until it is cleared to "0" manually. Manual setting of this flag position "1" is prohibited.

- VDET bit

Voltage detection flag bit; When the power supply voltage is detected to drop below 2.2V, causing the temperature compensation circuit to not work properly, this bit is set to "1". This flag bit will remain as "1" until it is cleared to "0" manually. Manual setting of this flag position "1" is prohibited.

- XST bit

The XST flag indicates oscillation stop. When detected, it's set to 1 which can be manually clear only and no manual set allowed. Defaults to 1 on power-up, prompting users to do time configuration. This bit can be cleared only via IIC after configuration. Remains 0 until next stop event. Ensures system stability.

- EN_DET bit

Oscillation Stop Detection Function Control Bit: When this bit is set to 1, the oscillation stop detection function is enabled. When set to 0, the function is disabled, which can save 50nA of current consumption. The default state of this control bit upon power-up is 1.

- RESET

When RESET is set to "1", the sub-second register is reset and the clock stops; Temperature compensation and VLF/VDET voltage detection function fail.

The RESET bit set to "1" will reset to "0" under the following three conditions: when the IIC termination condition is detected, when the restart condition is detected, or when the IIC bus is reset after 0.95S. At the same time, the VLF/VDET flag bit clears "0" and resets the power supply voltage detection function.

9.2.6 Frequency Accuracy Adjust Register（Reg 1A）

Output frequency can adjusted by Register 1Ah to realize more timer accuracy. The frequency adjust step can refer to table.

Table 10- 6 Frequency adjust step

OFS3	OFS2	OFS1	OFS0	Offset Value (ppm)
0	0	0	0	0.00
0	0	0	1	-0.55
0	0	1	0	-1.10
0	0	1	1	-1.65
0	1	0	0	-2.20
0	1	0	1	-2.75
0	1	1	0	-3.30
0	1	1	1	-3.85
1	0	0	0	4.40
1	0	0	1	3.85
1	0	1	0	3.30
1	0	1	1	2.75
1	1	0	0	2.20
1	1	0	1	1.65
1	1	1	0	1.10
1	1	1	1	0.55

9.2.7 Power Supply and Battery Management Registers（reg 19）

table 9- 9 Power Supply and Battery Management Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	PW Control	CHGEN	INIEN				SWSEL	SMPT1	SMPT0

- CHGEN bit

Charging Function Control Bit: When CHGEN=1, the charging function is enabled; when CHGEN=0, the charging function is disabled.

- INIEN bit

Automatic Power Supply Switching Function Switch Bit: When INIEN=1, the automatic power supply switching switch is enabled; when INIEN=0, the automatic power supply switching switch is disabled.

- SWSEL bit

Automatic Power Supply Switching Function Switch: When INIEN=1, the automatic power supply switching switch is enabled; when INIEN=0, the automatic power supply switching switch is disabled.

- SMPT1，SMPT0 bit

Control the size of the power supply detection window， choose in 300μs/600μs/2ms/256ms。

10 Power Supply function

The JXR131 features dual power supply functionality, allowing for configurable automatic switching between the two power sources. Additionally, the main power supply can provide trickle charging for the backup power source.

10.1 Relevant reg

The following table outlines the specific operation methods for control bit.

table 10- 1 Power supply control table

INIEN	CHGEN	SWSEL	SW1	Description
0	X	0	OFF（0）	Initial state. Single power supply
		1	ON（1）	------
1	0	X	Non-rechargeable battery serving as backup battery	Automatically control the switch state based on power supply detection results
	1		rechargeable battery serving as backup battery	

10.2 Power detection module

To fulfill the related functions of dual power supply control, the chip is equipped with two independent power detection units. One is used to detect whether the rechargeable battery is fully charged, and the other is used to determine if the main power supply voltage is higher than the backup power supply.

table 10- 2 power control symbols

Symbol Name	Description
VD2	Compare the voltage between V_{BAT} and V_{FULL}，while V_{BAT} is larger than V_{FULL}，output 1
VD3	Compare the voltage between V_{BAT} and V_{DD}，while V_{BAT} is larger than V_{FULL}，output 1

10.3 Initial state upon power-on

The default power-up state of the power management section is as shown in the diagram below. Vbat is directly connected to the RTC power supply terminal, while VDD is connected to the RTC power supply terminal through a diode. Therefore, when using a single power supply, it is recommended to power the system through VBAT or to short-circuit VBAT and VDD.

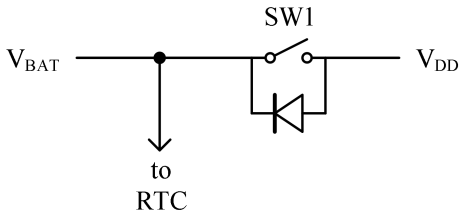


图 10- 1 Initial state upon power-on

10.4 single power supply

When chip is powered by single power supply, it is advised that the user commit a short-circuit between VDD

and VBAT or power the chip by using VBAT

10.5 Non-rechargeable battery serving as backup battery

When the backup power source is a non-rechargeable battery, it is necessary to set INIEN to 1 to enable the automatic power supply switching function, and set CHGEN to 0 to disable the charging function.

table 10- 3 Non-rechargeable battery serving as backup battery

Power detection result	SW1	Power supply state
$V_{DD} > V_{BAT}$	ON	Powered by main battery
$V_{DD} < V_{BAT}$	OFF	Powered by backup battery

10.6 Rechargeable battery serving as backup battery

When a rechargeable battery is used as the backup power source, set INIEN to 1 to enable the automatic power supply switching function, and set CHGEN to 1 to enable the charging function. Based on the results of the two power supply detection units(V_{BAT} vs V_{DD}， V_{BAT} vs V_{FULL}), the power supply state will be switched automatically. Among them, VFULL represents the cutoff charging voltage for the backup power source. The control states of the switches are as follows in the table:

table 10- 4 rechargeable battery serving as backup battery

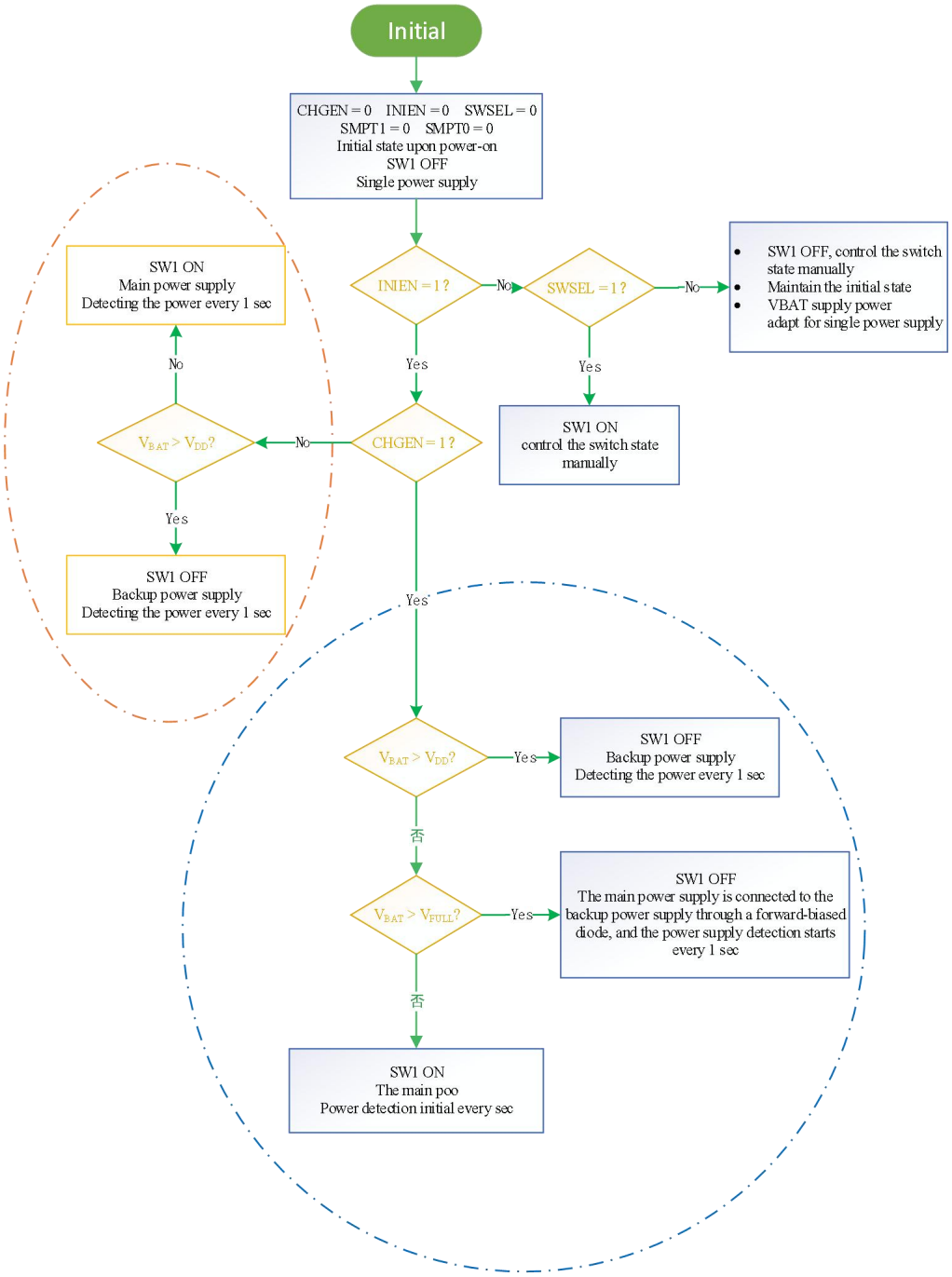
Power detection result		SW1	Charging state	Power supply state
$V_{DD} < V_{BAT}$		OFF	Stop charging	Powered by backup battery
$V_{DD} > V_{BAT}$	$V_{BAT} \geq V_{FULL}$	OFF	Stop charging	Powered by main battery
	$V_{BAT} < V_{FULL}$	ON	charging	Powered by main battery

During power supply detection, to ensure the accuracy of the detection results, it is necessary to disconnect SW1 for the detection process. The detection window is determined by SMPT1 and SMPT0.

table 10- 5 Power supply detection window

SMPT1	SMPT0	Detection window
0	0	300us *Default
0	1	600us
1	0	2ms
1	1	256ms

10.7 Process of power supply management



11 Interrupt function

11.1. Alarm interrupt

Alarm interrupts can generate an interrupt event for a set week, day, hour, or minute.

11.2. Alarm Interrupt Timing

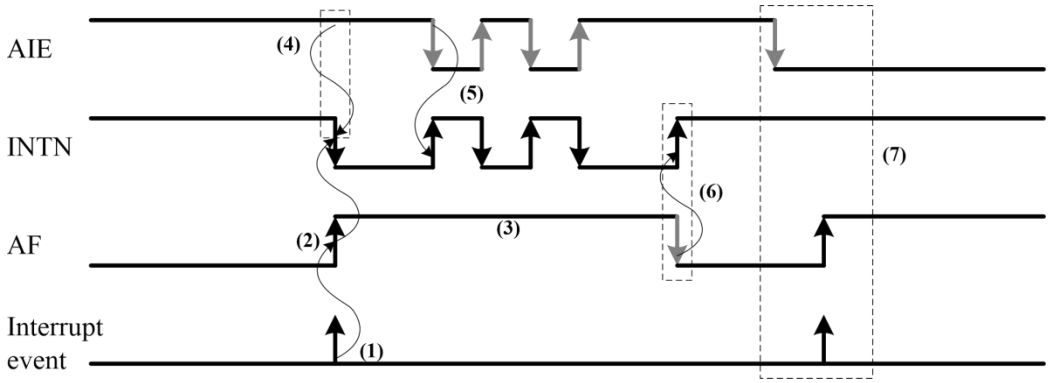


Figure 11- 1 Alarm interrupt sequence

(1) Set the hour, minute, date, or week corresponding to the alarm interruption. When the set time matches the current time (for details about the mapping, see Table 10-3), an interruption event is generated

(2) When the alarm interrupt event occurs, the AF flag bit is set to "1".

(3) The AF register will remain "1" until it is manually cleared to "0" via the IIC port.

(4) When the alarm interrupt event occurs, if AIE= "1", INTN outputs a low level; If AIE= "0", INTN remains Hi-Z

(5) If AIE is set to "0" during INTN= "0", INTN immediately returns to the Hi-Z state. AIE can be used to control the output state of INTN before the alarm interrupt event occurs and the AF register is cleared to "0"

(6) Clearing AF register "0" clears the alarm interrupt output, and INTN changes from "0" to Hi-Z status immediately

(7) If AIE= "0" when the alarm interrupt event occurs, INTN remains Hi-Z and does not output low, but the AF flag bit is set to "1".

11.2.1. Alarm interrupt related register

Table 11- 1 Alarm interrupt correlation register

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D or 1D	Extension	○	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	**AF**	○	○	XTS
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	**AIE**	○	EN_DET	RESET

- When configuring the alarm interrupt register, it is recommended to set AIE to "0" first to prevent unnecessary hardware interrupts during operation.
- WADA is used to select the alarm mode, when set to "1", daily alarm mode, when set to "0", weekly alarm mode.
- The occurrence of an alarm interruption event will set the AF flag position "1", which will remain "1" until it is set to "0" manually.
- When an alarm interrupt event occurs, AIE decides whether to generate an interrupt signal output (AIE= "1", then INTN= "0"; AIE= "0", then INTN=Hi-Z).
- An AE bit of "0" means that the corresponding register needs to be compared to a clock or calendar register; If the AE bit is "1", the corresponding register is not compared, that is, the register is always considered to match the corresponding clock or calendar register. Refer to the following example:

(1) When register 0A is set to "80", only the minute alarm and time alarm register need to be compared with the corresponding clock register, ignoring the day/date register; Therefore, as long as the hour register and the minute register match, an alarm interrupt event will be generated every day.

(2) 08, 09, 0A Setting the AE bits in all three registers to "1" will result in an alarm interrupt event every minute.

18

11.3. Fixed Cycle Interrupt Interrupt

Fixed period interrupts can generate interrupt events at a set period between 244.14 μs and 255min.

11.3.1. Timed Interrupt Timing

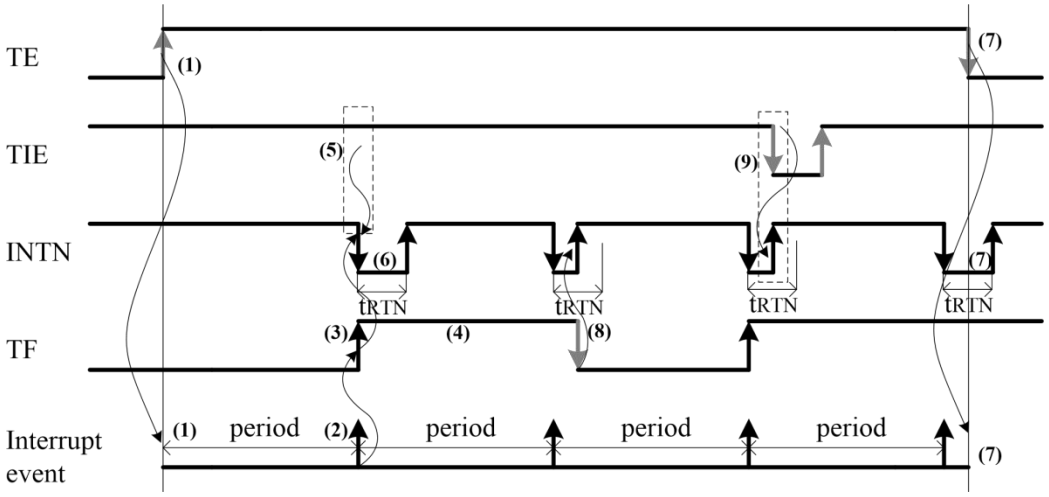


Figure 11- 2 Fixed-cycle Timer Interrupt Timing Chart

(1) When the TE bit is written to "1", the fixed period counter counts backwards from the preset value

(2) When the timer counter counts from 01h to 00h, an interrupt event is generated;Counter 0F resets to the preset value and continues the next backward count

(3) TF register is set to "1" when timed interrupt event occurs

(4) The TF register will remain in the "1" state until it is manually cleared to "0" via the IIC port

(5) When the timing interrupt event occurs, if TIE= "1", INTN outputs a low level; If TIE= "0", INTN remains Hi-Z

(6) INTN outputs the low level for t_{RTN}, and then automatically restores the Hi-Z state until the next interruption signal output,RTN as shown in Table11-3.

(7) When TE bit writes "0", timing counter stops counting and INTN outputs Hi-Z (If TE write "0" occurs during INTN= "0", after t_{RTN} , INTN restores Hi-Z state)

(8) When TE bit writes "0", timing counter stops counting and INTN outputs Hi-Z (If TE write "0" occurs during INTN= "0", after tRTN , INTN restores Hi-Z state)

(9) If TF is cleared "0" during INTN= "0", INTN immediately returns to the Hi-Z state (9)When TIE is written to "0", INTN immediately returns to Hi-Z

11.3.2. Fixed cycle interrupt related register

Table 11- 2 Fixed cycle interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	TimerCounter0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C or 1C	TimerCounter1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D or 1D	Extension	○	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0E or 1E	Flag	○	○	UF	**TF**	AF	○		XST
0F or 1F	Control	CSEL1	CSEL0	UIE	**TIE**	AIE	○	EN_DET	RESET

- When configuring the timed interrupt register, it is recommended to set TE and TIE to "0" first to prevent unnecessary hardware interrupts during operation.
- TSEL1 and TSEL0 are used to set the inverted count period of the fixed period interrupt. The automatic reset time of the interrupt signal on the INTN pin is related to the inverted count period.

Fixed period interrupt count cycle and automatic reset time

TSEL[1]	TSEL[0]	Source clock	Auto reset time
0	0	4.096kHz	0.122mS
0	1	64Hz	7.8125mS
1	0	1Hz	7.8125mS
1	1	1/60Hz	7.8125mS

- Register 0B or 1B, 0C or 1C sets the default value of the counter (001h~FFFh), which generates a fixed period interrupt event when the counter counts backwards to 000h in the counting period set by TSEL.
- TE is the enable control bit of the fixed period counter. When TE= "1", the counter starts to count backwards; When TE= "0", the counter stops counting and terminates the fixed period interrupt function.
- The occurrence of a fixed period interrupt event will mark TF position "1", which will remain "1" until it is manually set to "0".
- When a fixed period interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE= "1", then INTN= "0"; TIE= "0", then INTN=Hi-Z).

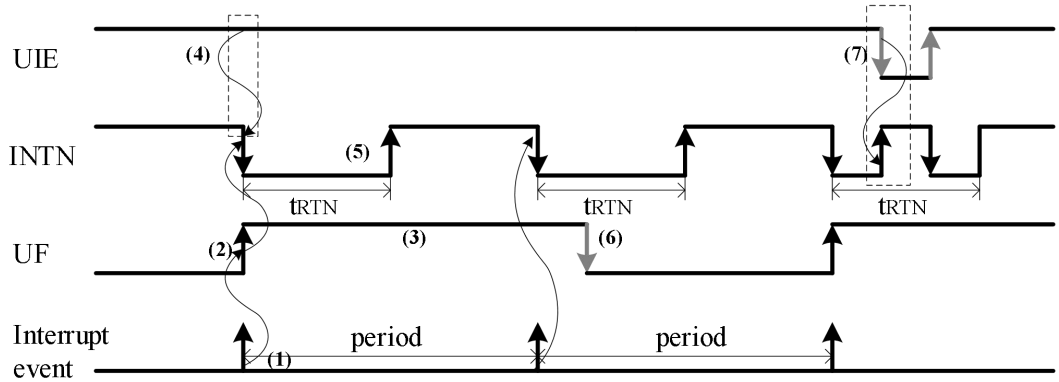
Table 10-4 Samples of fixed cycle interrupt cycle

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
……	……	……	……	……
2048	500ms	32s	2048s	2048min
……	……	……	……	……
4095	0.9998s	63.984s	4095s	4095min

11.4. Time Update Interrupt Function

Fixed period interrupts can generate interrupt alarm events at a fixed period between 244.14 μS and 4095min.

11.4.1. Fixed cycle interrupt timing



(1) The USEL register determines whether the chip is in a second update interrupt or minute update interrupt state, and generates a time update interrupt event when the corresponding second register or minute register is updated.

(2) When the time update interrupt event occurs, the UF register is set to "1".

(3) The UF register will remain in the "1" state until it is cleared to "0" manually.

(4) INTN outputs a low level if UIE= "1" when the time update interrupt event occurs; If UIE= "0", INTN remains Hi-Z.

(5) INTN outputs a low level for tRTN, after which it automatically returns to Hi-Z status until the next interruption signal output.

(6) If UF is cleared to "0" during INTN= "0", INTN returns to Hi-Z after tRTN time.

(7) If UIE is set to "0" during INTN= "0", INTN immediately restores the Hi-Z state and the interrupt signal output ends. If UIE is written as "1" again during tRTN, INTN will remain in the Hi-Z state.

10.3.2 Time Update Interrupt related register

Time update interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	○	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	**UF**	TF	AF	○	○	VDET
0F or 1F	Control	CSEL1	CSEL0	**UIE**	TIE	AIE	○	EN_DET	RESET

- When configuring the time update interrupt register, it is recommended to set the UIE to"0" first to prevent unnecessary hardware interrupts during operation.
- The USEL signal is used to set the interrupt mode to second update or minute update.

Time update interrupt mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event will leave the UF flag position "1", which will remain "1" until it is manually cleared to "0".
- When the time update interrupt event occurs, UIE decides whether to generate an interrupt signal output (UIE= "1", then INTN= "0"; UIE= "0", then INTN=Hi-Z).

12 IIC bus interface

12.1. IIC bus features

IIC is a two-way communication interface, its signal line SDA and clock line SCL need to be connected to VDD through pull-up resistance; The port connected to the IIC bus must be open-drain structure in order to realize the line and connection of multiple devices.

12.2. Data Transmission

1bit of data can be transferred per SCL clock cycle. When sending data, the data on the SDA line changes during the SCL low; When receiving data, stable and effective data can be obtained from the data line SDA during the high level of SCL.

12.3. Start condition and end condition

SCL and SDA remain high when idle. When SCL is high, the falling edge of SDA serves as the starting condition for IIC communication. During the high level of SCL, the rising edge of SDA is used as the termination condition of IIC communication.

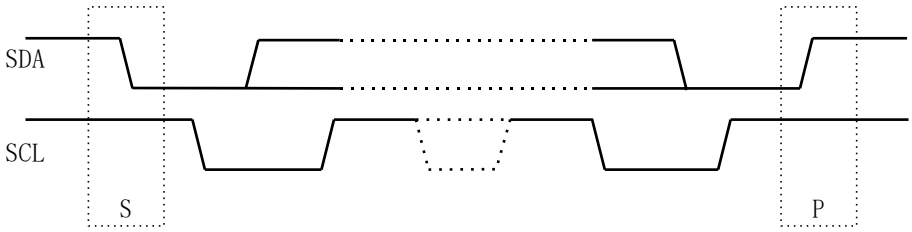


Figure 12- 1 IIC start condition and end condition

12.4. Device selection (from address)

The IIC bus device has no chip selection signal, the master device selects the corresponding slave device by sending a unique fixed device number (from the address), and the selected slave device sends a reply signal to establish communication with the master device.

The slave address includes 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2). The slave address of JXR131 is "0110010". During communication, the slave address and R/W select bits are sent as 8bit data.

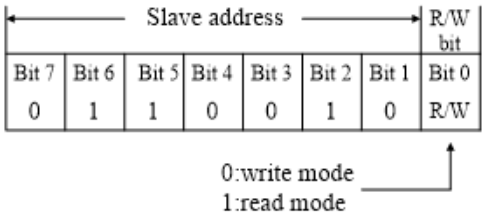


Figure 12- 2 IIC schematic from the address

12.5. System configuration

The device that controls data transmission is called the "master device" and the device controlled by the master device is called the "slave device"; The device that sends the data is called the "sending end" and the device that receives the data is called the "receiving end."

In a JXR131 system, the CPU or other control device is the primary device, and the

JXR131 chip itself is the secondary device; Both the master and slave devices can be used as sending or receiving ends.

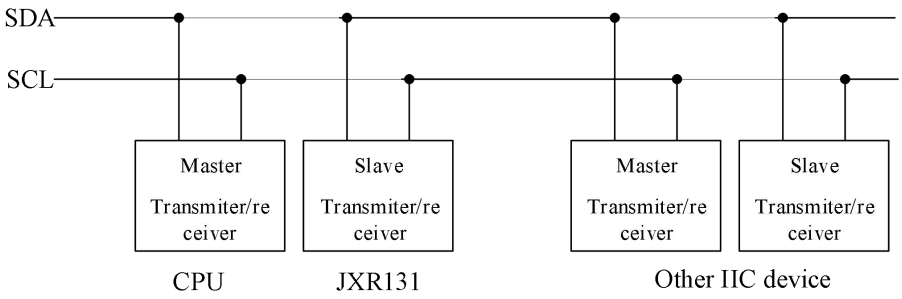


Figure 12- 3 IIC system configuration

12.6. Answer signal

The IIC bus has no limit on the number of bytes that can be transferred between the start and end conditions. After each byte of data is transferred, the sender releases the SDA bus and provides an SCL clock to receive the reply signal. If the receiver successfully receives 8 bits of data, the SDA must be set to "0" after the end of the clock for transmitting the last 1bit of data, and the sender will use this low level as the response signal of successful data transmission; After 1 clock cycle, the receiving end releases the SDA bus, ready to receive new data.

The IIC bus terminates the data transfer when the following conditions are met:

(1) When the master device acts as the sender, it sends the termination condition after receiving the reply signal from the slave device.

(2) When the master device acts as the receiver, after successfully receiving 8 bits of data, it sends a "1" as the reply signal and sends the termination condition immediately.

12.7. IIC bus control

This section describes the IIC bus communication timing for the CPU as the master device and the JXR131 as the slave device.

12.7.1. Specify address write operations

JXR131 has the address automatic increment function, after setting the operation address, only need to send data continuously, the address bit can be automatically incremented.

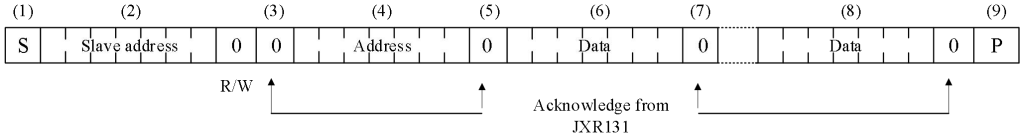


Figure 12- 4 Specify the address write operation

(1) CPU send start condition [S].

(2) The CPU sends JXR131 from the address and is set to write mode via R/W bit.

(3) The JXR131 generates an answer signal.

(4) The CPU sends the write register address to JXR131.

(5) The JXR131 generates an answer signal.

(6) The CPU sends data to the register corresponding to the address specified in (4).

(7) The JXR131 generates an answer signal.

(8) Repeat the process (6) (7) and the address of the write register in JXR131 will automatically increment.

(9) CPU send termination condition [P].

12.7.2. Specify an address read operation

After writing to the register, the CPU can read the register data by setting the read mode.

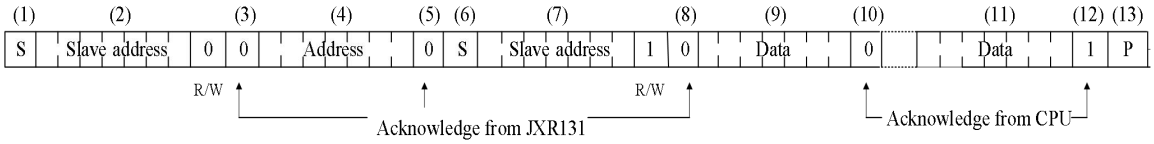


Figure 12- 5 specifies the address read operation

(1) CPU send start condition [S].

(2) The CPU sends JXR131 from the address and is set to write mode via R/W bit.

(3) The JXR131 generates an answer signal.

(4) The CPU sends the read register address to the JXR131.

(5) The JXR131 generates an answer signal.

(6) The CPU re-sends the start condition.

(7) The CPU sends JXR131 from the address and is set to read mode via R/W bits.

(8) JXR131 generates a response signal; After that, the CPU acts as the receiver and the JXR131 acts as the transmitter.

(9) The JXR131 sends the data in the register corresponding to the address specified in (4) (10)The CPU sends a reply signal to the JXR131.

(10) Repeat the process (9) (10) and the address of the read register in JXR131 will automatically increment.

(11) The CPU does not send a reply signal to JXR131; The JXR131 switches to the IIC data receiver.

(12) CPU send termination condition [P].

12.7.3. Address read operation not specified

The master device goes directly into read mode to read the contents of all registers from the device. The read operation address is the last IIC operation address +1.

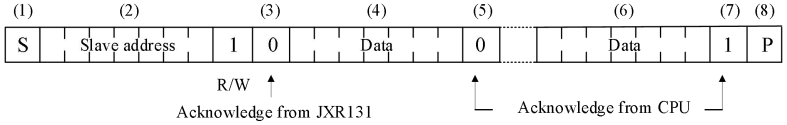


Figure 12- 6 does not specify the address read operation

(1) CPU send start condition [S].

(2) The CPU sends the JXR131 slave address and is set to read mode via R/W bit. The JXR131 generates an answer signal; After that, the CPU acts as the receiver and the JXR131 acts as the transmitter.

(3) The JXR131 automatically increments the register address and sends the register data.

(4) The CPU sends a reply signal to the JXR131.

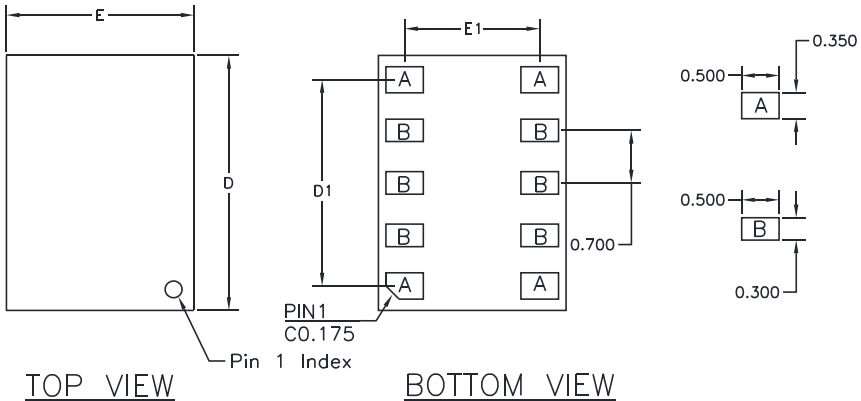
(5) Repeat the process (4) (5) and the address of the read register in JXR131 will automatically increment.

(6) The CPU does not send a reply signal to the JXR131; The JXR131 switches to the IIC data receiver.

(7) CPU send termination condition [P]

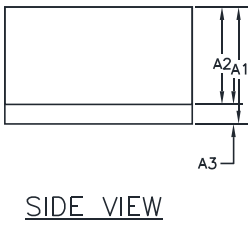
Appendix

Package size



Dimensional Ref.

REF.	Min.	Nom.	Max.
A1	1.45	1.55	1.65
A2		1.30 BSC	
A3	0.16	0.26	0.36
D	3.20	3.40	3.60
E	2.30	2.50	2.70
D1		2.75 BSC	
E1		1.80 BSC	



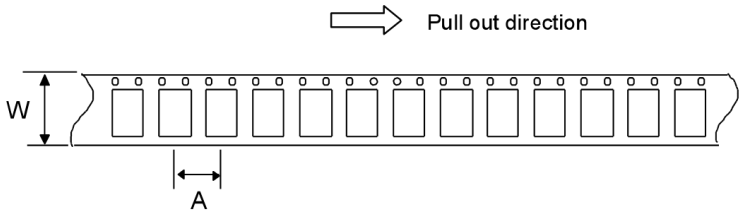
Unit：mm

Packing specification

Emboss Taping (TE2)

Symbol	LGA10
A	4
W	12

Unit : mm



Symbol	LGA10
A	330
W	12.4

Unit : mm