JXR151T User Manual

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Catalogue

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1 Overview

JXR151T is a high accuracy, real-time clock module with IIC interface, which includes a 32.768kHz DTCXO; The minimum timing unit is second, can realize automatic leap year correction, and can provide alarm function, fixed-cycle Timer Interrupt function, time update interrupt function and 32.768KHz/1024Hz/1Hz clock output function.

2 Characteristics

- Built-in 32.768kHz DTCXO，High Stability
- Operating temperature range: -40℃~85℃
- Supports IIC-Bus's high-speed mode (Up to 400 kHz)
- Alarm interrupt function for day, date, hour, and minute settings
- Fixed-Cycle Timer Interrupt
- Time Update Interrupt(Seconds, minutes)
- 32.768kHz/1024Hz/1Hz clock output with enable control
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 2.2V ~ 5.5V
- Wide time-keeping voltage range: 1.8V ~ 5.5V
- Low current power consumption: 2.3μA@3V(Typ)

3 Block Diagram

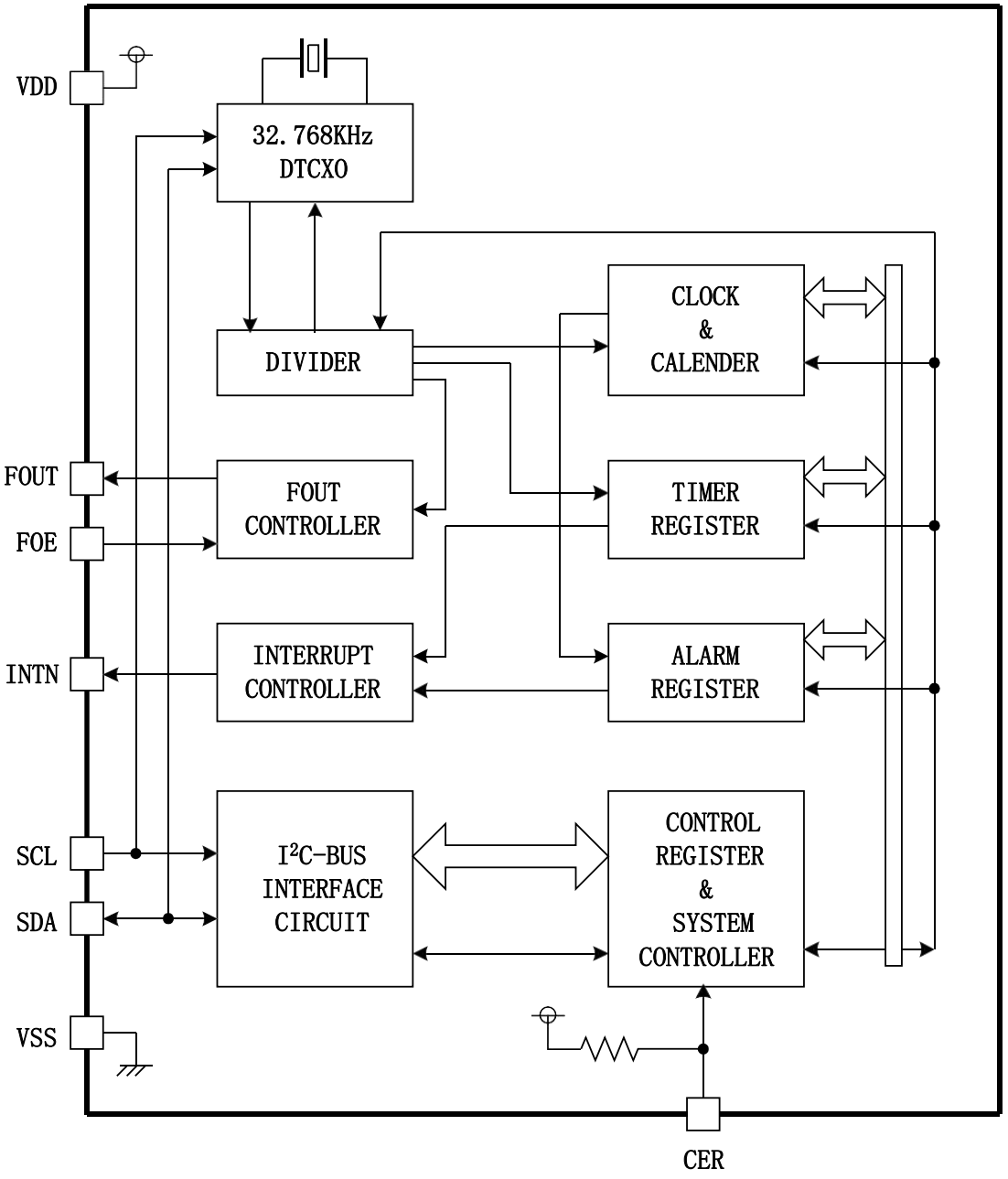


Figure 3-1 JXR151T system block diagram

4 Terminal description

4.1 Package Form

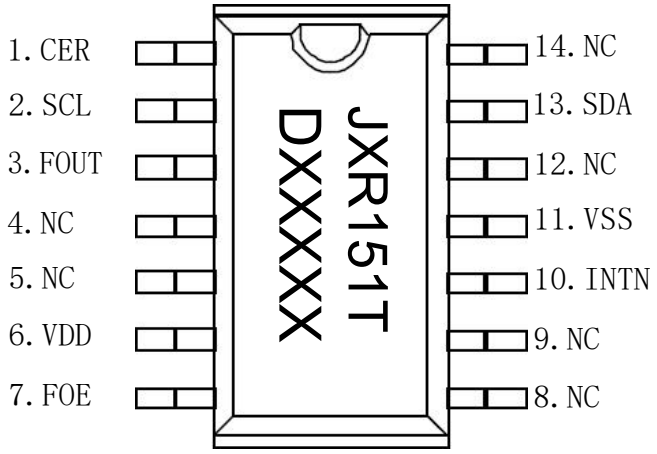


Figure 4-1 JXR151T package form

4.2 Pin Function

Table 4-1 JXR151T Pin Desciption

Pin name	I/O	Function
1. CER	IN	Use by the manufacture for testing. (Do not connect externally.)
2. SCL	IN	This is the serial clock input pin for IIC Bus communications.
3. FOUT	OUT	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
4/5/8/9/12/14:NC	--	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.
6.VDD	POWER	This pin is connected to a positive power supply.
7. FOE	IN	The FOUT output enable pin, which should be connected to a fixed potential. When the FOUT output function is not utilized, this pin should be connected to ground potential.
10.INTN	OUT	This pins is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
11.VSS	GROUND	This pin is connected to a ground.
13.SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2 C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.

5 Absolute Maximum ratings

Table 5-1 Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply voltag*1	V_{DD}	Voltage between VDD and VSS	-0.5 to 6.5	V
Input voltage*7, *2	V_{IN}	FOE, SCL, SDA pins	-0.5 to V_{DD}+0.3	V
Output voltage*1, *2	V_{OUT}	FOUT, SDA, INTN pins	-0.5 to V_{DD}+0.3	V
Storage temperature	T_{STG}	Store separately, unpacked	-55 to 125	ºC

*1: Each electrical indicator shall not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of relevant parameters, reliability reduction and even chip failure.

*2:This V_{DD} refers to the range of V_{DD} under recommended operating conditions.

6 Recommended operating conditions

Table 6-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Interface voltage	1.8	3.0	5.5	V
Temp. Compensation voltage	V_{TEM}	Temperature compensation voltage	2.2	3.0	5.5	V
Clock supply voltage	V_{CLK}	operating voltage of Oscillator module	1.8	3.0	5.5	V
Operating temperaturec range	T_{OPR}	---	-40	25	85	ºC

* Any operation beyond the recommended range in the above table can greatly affect the reliability of the chip.

7 Frequency characteristics

Table 7-1 Frequency Characteristics

Item	symbol	Condition		MIN	TYP	MAX	Unit
Frequency stability	Δf/f	UA	Ta=0 ºC~50 ºC, V_{DD}=3.0V			±1.5	$\times10^{-6}$
			Ta=-40 ºC~85 ºC, V_{DD}=3.0V			±3.0	
		UB	Ta=0 ºC~50 ºC, V_{DD}=3.0V			±3.0	
			Ta=-40 ºC~85 ºC, V_{DD}=3.0V			±5.0	
		UC	Ta=0 ºC~50 ºC, V_{DD}=3.0V			±3.8	
			Ta=-30 ºC~70 ºC, V_{DD}=3.0V			±5.0	
Voltage coefficient	Δf/f/V	Ta=25 ºC, V_{DD}=2.2V~5.5V			±0.5	±1.0	$\times10^{-6}$/V
Oscillation start time	T_{STA}	Ta=25 ºC, V_{DD}=1.8V				0.9	s
		Ta=-40ºC~85ºC,V_{DD}=1.8V~5.5V				2.0	
Aging	fa	Ta=25 ºC, V_{DD}=3.0V, first year				±1.0	$\times10^{-6}$/year

8 Electrical characteristics

8.1 DC Characteristics

Table 8-1 DC Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{DD1}	FOE=GND FOUT=Hi-Z	V_{DD}=5V		2.4	3.2	μA
	I_{DD2}		V_{DD}=3V		2.3	3.0	
Current consumption	I_{DD3}	FOE=VDD FOUT=32.768KHz CL=0pF	V_{DD}=5V		3.6		μA
	I_{DD4}		V_{DD}=3V		3.0		
Current consumption	I_{DD5}	FOE=VDD FOUT=32.768KHz CL=30pF	V_{DD}=5V		7.5		μA
	I_{DD6}		V_{DD}=3V		6.2		
Current consumption	I_{DD7}	During IIC communication, V_{DD}=5V				700	μA
High-level input voltage	V_{IH}	FOE, SCL, SDA pins	V_{DD}=2.2V~5.5V	0.7*V_{DD}		V_{DD}	V
Low-level input Voltage	V_{IL}	FOE, SCL, SDA pins	V_{DD}=2.2V~5.5V	0		0.3*V_{DD}	V
High-level output voltage	V_{OH}	FOUT pin	V_{DD}≥3V I_{OL}=-3mA	V_{DD}-0.3		V_{DD}	V
Low-level output voltage	V_{OL}	FOUT pins	V_{DD}≥3V I_{OL}=-3mA	GND		GND+0.3	V
		SDA, INTN pin	V_{DD}≥2V I_{OL}=-3mA	GND		GND+0.3	V
Input leakage current	I_{LK}	FOE, SCL, SDA, V_{IN}=V_{DD} or GND		-0.3		0.3	μA
Output leakage current	I_{OZ}	INTN, FOUT, SDA, V_{IN}=V_{DD} or GND		-0.3		0.3	μA

8.2 AC Characteristics

Table 8-2 AC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	---			400	KHz
Start condition setup time	$t_{SU;STA}$	---	0.6			μS
Start condition hold time	$t_{HD;STA}$	---	0.6			μS
Data setup time	$t_{SU;DAT}$	---	100			nS
Data hold time	$t_{HD;DAT}$	---	0			nS
Stop condition setup time	$t_{SU;STO}$	---	0.6			μS
Bus idle time	t_{BUF}	Between start condition and stop condition	1.3			μS
Time when SCL = "L"	t_{LOW}	---	1			μS
Time when SCL = "H"	t_{HIGH}	---	1			μS
Rise time for SCL and SDA	t_r	---			0.3	μS
Fall time for SCL and SDA	t_f	---			0.3	μS
Allowable spike time on bus	t_{SP}	---			50	nS
FOUT duty	Duty	50% of VDD level	40	50	60	%

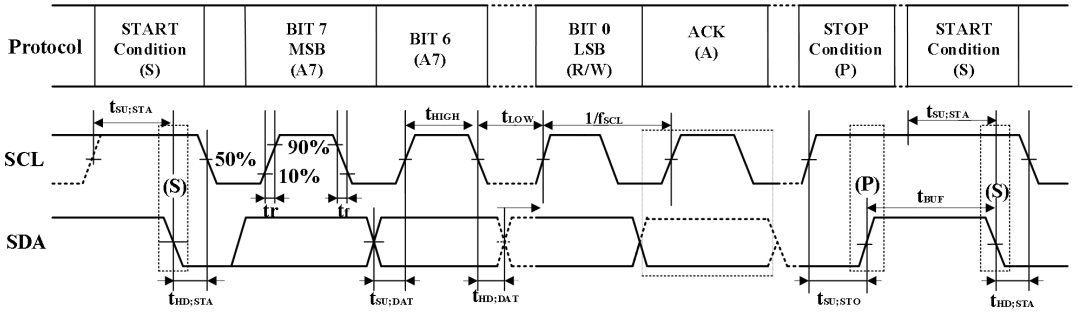


Figure 8-1 IIC timing legend

* The IIC data transfer is located between the start condition and the end condition, and the data transfer operation must be completed within 0.95S time, after which the IIC bus will be reset by the internal timer.

9 Registers

9.1 Register summary table

Table 9-1 Register Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	SEC	○	40	20	10	8	4	2	1
1	MIN	○	40	20	10	8	4	2	1
2	HOUR	○	○	20	10	8	4	2	1
3	WEEK	○	6	5	4	3	2	1	0
4	DAY	○	○	20	10	8	4	2	1
5	MONTH	○	○	○	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1
7	RAM	●	●	●	●	●	●	●	●
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	●	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
B	Timer Counter 0	128	64	32	16	8	4	2	1
C	Timer Counter 1	●	●	●	●	2048	1024	512	256
D	Extension Register	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET

* Make sure to write a legal value to the calendar clock register, otherwise the chip will not be able to perform the correct timing operation.

* Register bits marked with ○ are read-only bits and read values are "0"; Register bits marked with ● can be used as RAM to perform reading and writing operations.

*If the alarm interrupt function is not set (AIE= "0"), registers 8~A can be used as RAM.

*If the fixed period interrupt function (TE=TIE= "0") is not set, registers B, C can be used as RAM.

*UF, TF, AF, VLF, and VDET bits are only allowed to be written to "0".

*When the chip is powered on, the CSEL0 bit is preset to "1", FSEL1, FSEL0, CSEL1, VLF，UIE, TIE, AIE bits are preset to "0".

9.2 Details of Registers

9.2.1 Clock and calendar registers (registers 00~06 or 10~16)

- Data form

With the exception of the week register (register 3), the data is in BCD code form. For example, the value "0101 1001" in the second register means that it is currently 59 seconds.

The timing mode is fixed to the 24-hour system.

- Year register and leap year

The year register ranges from 00 to 99, and then returns to 00 after 99; The year is a leap year when the value represented by the register is divisible by 4. The calendar is valid from 2000 to 2099.

- Week Register

The week register has a total of 7 significant bits (bit0 to bit6), and each significant bit represents a day from Monday to Sunday, so only 1 bit of the register is allowed to be "1".

Table 9-2 Week registers table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	week
0	0	0	0	0	0	1	Sun.
0	0	0	0	0	1	0	Mon.
0	0	0	0	1	0	0	Tue.
0	0	0	1	0	0	0	Wed.
0	0	1	0	0	0	0	Thu.
0	1	0	0	0	0	0	Fri.
1	0	0	0	0	0	0	Sat.

9.2.2 Alarm register (Register08~0A)

The alarm can be set to X hours X minutes on X days of the week or X hours X minutes on X days of the month (week alarm mode and day alarm mode), and the alarm mode can be set via the WADA bit of register D.

Each Alarm register has AE (Alarm Enable) bits (bit7). When the AE bit of an alarm register is "0", the set value of the register needs to be compared with the corresponding timer register. When the value is consistent, the output alarm is interrupted; If the AE bit is "1", the corresponding alarm register value is ignored, that is, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is consistent with the corresponding timing register value.

When the WEEK ALARM mode is selected, several days of the week can be selected at the same time, that is, the week alarm function bit0 to bit6 in register A can have several bits of "1" at the same time. Refer to Table 9-3 for the corresponding relationship in week alarm mode.

Table 9-3 Week alarm mode register A table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A	Week alarm	Sat.	Fri	Thu	Wed.	Tue	Mon	Sun.

9.2.3 Fixed cycle counter control register (register B , C)

These two registers are used to set the preset backcount value of the fixed period interrupt. When the value in the above two registers changes from 001h to 000h, the fixed period interrupt event occurs, TF is set to "1" and INTN outputs a low level (if TIE is "1"); The B, C registers are then reset to the preset value and the countdown process is restarted.

9.2.4 Control register and Flag register (registers 0D~0F or1D~1F)

- WADA bits

  Alarm Interrupt mode selection bit, when set to "1", for daily alarm mode, when set to "0", for weekly alarm mode.

- USEL bit

  The period used to set the time update interrupt; The bit is an indefinite value when the chip is powered on, and needs to be manually configured during use.

Table 9-4 Time Update Interrupt mode selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

  When the position is "1", the counter with fixed period interruption starts to count backwards, and when it is set to "0", it stops counting backwards.

- FSEL bit

  Set the output frequency of the FOUT port. For details, see Table 9-5. After the chip is powered on, the default value is "00".

Table 9-5 FOUT output frequency selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768KHz *Default
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

- TSELbit

  The counting period used to set the fixed period interrupt.

Table 9-6 Fixed cycle interrupt count cycle selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF，TF，UF bit

  They are alarm interrupt, fixed period interrupt, time update interrupt flag bits; When the above interrupt event occurs, the corresponding flag bit is set to "1". The flag bit will remain as "1" until it is cleared to "0" manually. Do not manually set the flag position to "1".

- AIE，TIE，UIE bit

  They are used to set the interrupt signal output on the INTN pin when alarm interrupt, fixed period interrupt, time update interrupt event occurs; The power-on default value of the three bits is "0".

  The interrupt signal output on the INTN pin is alarm interrupt, fixed period interrupt, time update interrupt logic and, through the interrupt flag bit to judge the specific interrupt situation and determine the interrupt signal output.

- VLF bit

  Low voltage detection flag bit; This bit is set to "1" when the power supply voltage is detected to drop below 1.8V, causing the clock circuit to not work properly, or when the power-on reset signal is detected. This flag bit will remain as "1" until it is cleared to "0" manually. Manual setting of this flag position "1" is prohibited.

- VDET bit

  Voltage detection flag bit; When the power supply voltage is detected to drop below 2.2V, causing the temperature compensation circuit to not work properly, this bit is set to "1". This flag bit will remain as "1" until it is cleared to "0" manually. Manual setting of this flag position "1" is prohibited.

- CSEL bit

  Used to set the time interval for the temperature compensation circuit to start; When the chip is powered on, the default value is "01" (2S).

Table 9-7 Selection of warming interval

CSEL1	CSEL0	Operation interval
0	0	0.5S
0	1	2S *Default
1	0	10S
1	1	30S

- RESET bit

When RESET is set to "1", the sub-second register is reset and the clock stops; Temperature compensation and VLF/VDET voltage detection function fail.

The RESET bit set to "1" will reset to "0" under the following three conditions: when the IIC termination condition is detected, when the restart condition is detected, or when the IIC bus is reset after 0.95S. At the same time, the VDET flag bit will be cleared to "0", while the VLF flag bit will be cleared to “1” and resets the power supply voltage detection function.

10 Interrupt Function

10.1 Alarm interrupt Function

Alarm interrupts can generate alarm interrupt events on a set week, day, hour, and minute.

10.1.1 Alarm interruption sequence

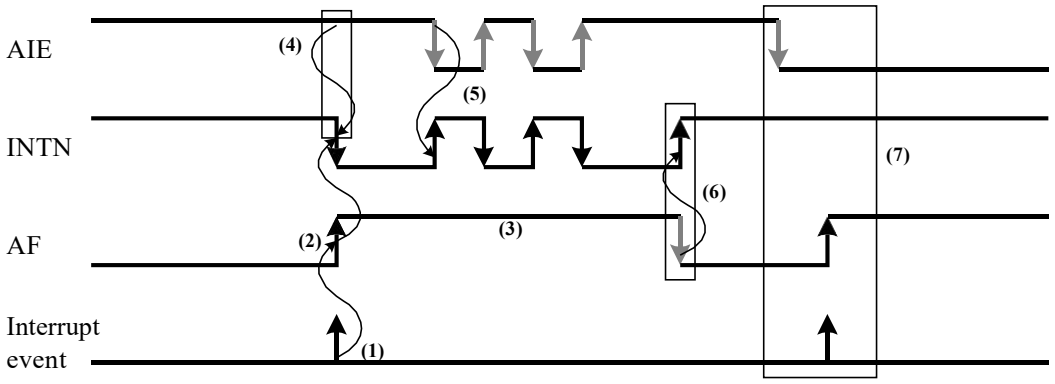


Figure 10-1 Alarm Interrupt Timing Chart

(1) Set the alarm interrupt corresponding hour, minute, date or week information and WADA register, when the set time matches the current time, the alarm interrupt event will be generated.

(2) When the alarm interrupt event occurs, the AF flag bit is set to "1".

(3) The AF register remains in the "1" state until it is manually cleared to "0".

(4) When the alarm interrupt event occurs, if AIE= "1", INTN output low; If AIE= "0", INTN remains Hi-Z.

(5) If AIE is set to "0" during INTN= "0", INTN immediately returns to the Hi-Z state. AIE can be used to control the output state of INTN before the alarm interrupt event occurs and the AF register is cleared to "0".

(6) Clearing the AF register to "0" clears the alarm interrupt output, and INTN changes from "0" to Hi-Z status immediately.

(7) If AIE= "0" when the alarm interrupt event occurs, INTN remains in Hi-Z state and does not output low.

10.1.2 Alarm interrupt related register

Table 10-1 Alarm Interrupt related registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	●	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
D	Extension Register	○	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

- When configuring the alarm interrupt register, it is recommended to set AIE to "0" first to prevent unnecessary hardware interrupts during operation.
- WADA is used to select the alarm mode, when set to "1", daily alarm mode, when set to "0", weekly alarm mode.
- The occurrence of an alarm interruption event will set the AF flag position "1", which will remain "1" until it is set to "0" manually.
- When an alarm interrupt event occurs, AIE decides whether to generate an interrupt signal output (AIE= "1", then INTN= "0"; AIE= "0", then INTN=Hi-Z).
- An AE bit of "0" means that the corresponding register needs to be compared to a clock or calendar register; If the AE bit is "1", the corresponding register is not compared, that is, the register is always considered to match the corresponding clock or calendar register. Refer to the following example:

(1) When register A is set to "80", only the minute alarm and time alarm register need to be compared with the corresponding clock register, ignoring the day/date register; Therefore, as long as the hour register and the minute register match, an alarm interrupt event will be generated every day.

(2) 8, 9, A Setting the AE bits in all three registers to "1" will result in an alarm interrupt event every minute.

10.2 Fixed Cycle Interrupt Function

Fixed period interrupts can generate interrupt alarm events at a fixed period between 244.14 μS and 4095min.

10.2.1 Fixed cycle interrupt timing

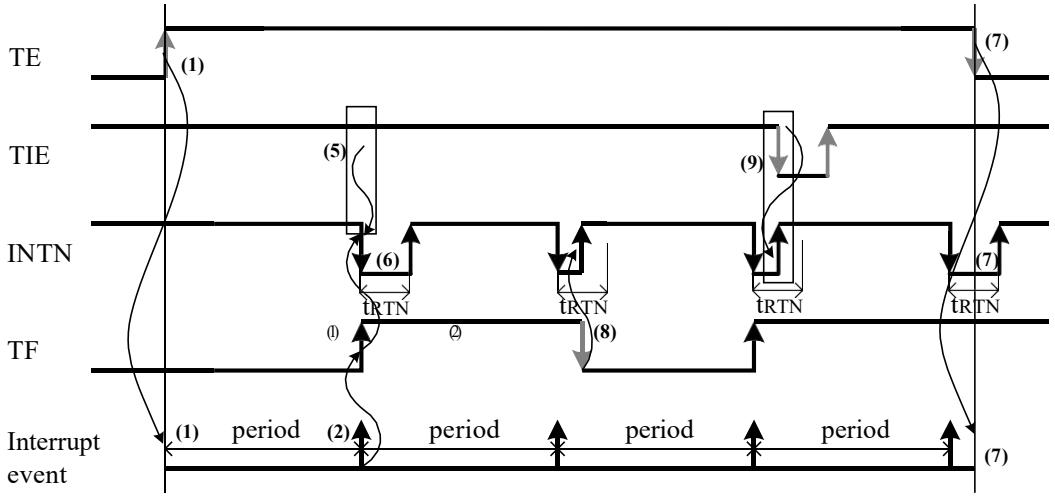


Figure 10-2 Fixed-cycle Timer Interrupt Timing Chart

(1) When the TE bit is written to "1", the fixed period counter counts backwards from the preset value.

(2) When the fixed period counter counts from 001h to 000h, an interrupt event is generated; The counter resets to a preset value and continues with the next count.

(3) The TF register is set to "1" when the fixed period interrupt event occurs.

(4) The TF register will remain in the "1" state until it is manually cleared to "0".

(5) When the fixed period interrupt event occurs, if TIE= "1", INTN outputs a low level; If TIE= "0", INTN remains Hi-Z.

(6) INTN outputs a low level for tRTN, after which it automatically returns to Hi-Z status until the next interruption signal output.

(7) When TE bit is written to "0", the fixed period counter stops counting and INTN outputs Hi-Z (if TE write "0" occurs during INTN= "0", INTN returns to Hi-Z status after tRTN time).

(8) If TF is cleared to "0" during INTN= "0", INTN immediately returns to Hi-Z status.

(9) When TIE is written to "0", INTN immediately returns to the Hi-Z state. If TIE is written to "1" again during tRTN, INTN will remain in Hi-Z.

10.2.2 Fixed cycle interrupt related register

Table 10-2 Fixed cycle interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C or 1C	Timer Counter 1	●	●	●	●	**2048**	**1024**	**512**	**256**
0D or 1D	Extension Register	○	WADA	USEL	**TE**	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag Register	○	○	UF	**TF**	AF	○	VLF	VDET
0F or 1F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	○	○	RESET

• When configuring the fixed-period interrupt register, you are advised to set TE and TIE to “0” first to prevent unnecessary hardware interrupts during operations.

• TSEL1 and TSEL0 are used to set the inverted count period of the fixed period interrupt. The automatic reset time of the interrupt signal on the INTN pin is related to the inverted count period.

Table 10-3 Fixed period interrupt count cycle and automatic reset time

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122mS
0	1	64Hz	7.8125mS
1	0	1Hz	7.8125mS
1	1	1/60Hz	7.8125mS

• Register B & C sets the default value of the counter (001h~FFFh), which generates a fixed period interrupt event when the counter counts backwards to 000h in the counting period set by TSEL.

• TE is the enable control bit of the fixed period counter. When TE= "1", the counter starts to count backwards; When TE= "0", the counter stops counting and terminates the fixed period interrupt function.

• The occurrence of a fixed period interrupt event will mark TF position "1", which will remain "1" until it is manually set to "0".

• When a fixed period interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE= "1", then INTN= "0"; TIE= "0", then INTN=Hi-Z).

Table 10-4 Samples of fixed cycle interrupt cycle

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14 μ S	15.625mS	1S	1min
……	……	……	……	……
2048	500mS	32S	2048S	2048min
……	……	……	……	……
4095	0.9998S	63.984S	4095S	4095min

10.3 Time Update Interrupt Function

Depending on the set value, a time update interrupt generates an interrupt alarm event with a second update or minute update.

10.3.1 Time update interrupt timing

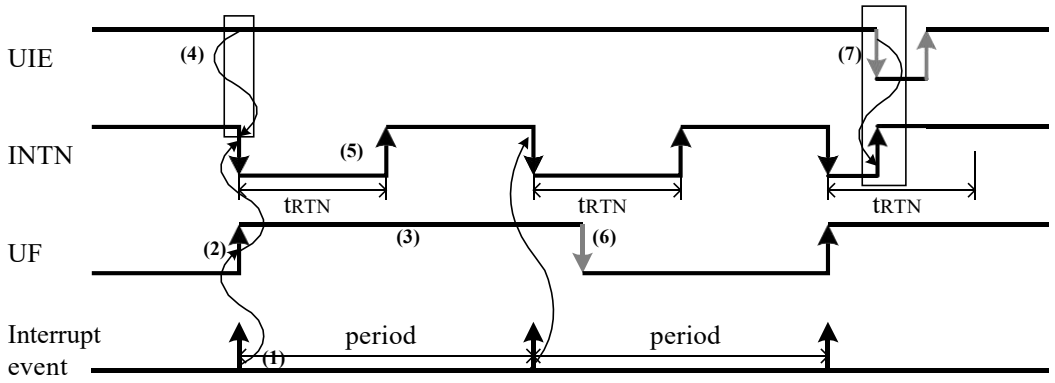


Figure 10-3 Time Update Interrupt Timing Chart

(1) The USEL register determines whether the chip is in a second update interrupt or minute update interrupt state, and generates a time update interrupt event when the corresponding second register or minute register is updated.

(2) When the time update interrupt event occurs, the UF register is set to "1".

(3) The UF register will remain in the "1" state until it is cleared to "0" manually.

(4) INTN outputs a low level if UIE= "1" when the time update interrupt event occurs; If UIE= "0", INTN remains Hi-Z.

(5) INTN outputs a low level for tRTN, after which it automatically returns to Hi-Z status until the next interruption signal output.

(6) If UF is cleared to "0" during INTN= "0", INTN returns to Hi-Z after tRTN time.

(7) If UIE is set to "0" during INTN= "0", INTN immediately restores the Hi-Z state and the interrupt signal output ends. If UIE is written as "1" again during tRTN, INTN will remain in the Hi-Z state.

10.3.2 Time Update Interrupt related register

Table 10-5 Time update interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D	Extension Register	○	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

- When configuring the time update interrupt register, it is recommended to set the UIE to"0" first to prevent unnecessary hardware interrupts during operation.
- The USEL signal is used to set the interrupt mode to second update or minute update.

Table 10-6 Time update interrupt mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event will leave the UF flag position "1", which will remain "1" until it is manually cleared to "0".
- When the time update interrupt event occurs, UIE decides whether to generate an interrupt signal output (UIE= "1", then INTN= "0"; UIE= "0", then INTN=Hi-Z).

11 IIC bus interface

11.1 IIC bus features

IIC is a two-way communication interface, its signal line SDA and clock line SCL need to be connected to VDD through pull-up resistance; The port connected to the IIC bus must be open-drain structure in order to realize the line and connection of multiple devices.

11.2 Data Tansfer

1bit of data can be transferred per SCL clock cycle. When sending data, the data on the SDA line changes during the SCL low; When receiving data, stable and effective data can be obtained from the data line SDA during the high level of SCL.

11.3 Starting and Stopping conditions

SCL and SDA remain high when idle. When SCL is high, the falling edge of SDA is used as the starting condition for IIC communication. During the high level of SCL, the rising edge of SDA is used as the termination condition of IIC communication.

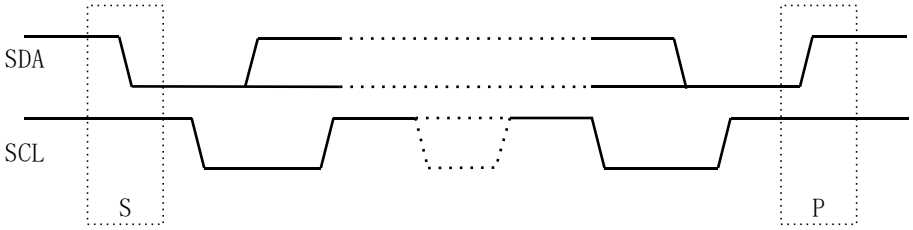


Figure 11-1 IIC starting condition and stopping condition

11.4 Device selection (from address)

The IIC bus device has no chip selection signal, the master device selects the corresponding slave device by sending a unique fixed device number (from the address), and the selected slave device sends a reply signal to establish communication with the master device.

The slave address includes 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2). The slave address of the JXR151T is "0110010". During communication, the slave address and R/W select bits are sent as 8bit data.

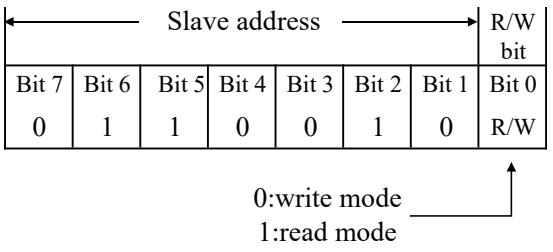


Figure 11-2 IIC schematic drawing from address

11.5 System configuration

The device that controls data transmission is called the "master device" and the device controlled by the master device is called the "slave device"; The device that sends the data is called the "sending end" and the device that receives the data is called the "receiving end."

In a JXR151T system, the CPU or other control device is the primary device, and the JXR151T chip itself is the secondary device; Both the master and slave devices can be used as the sending or receiving end.

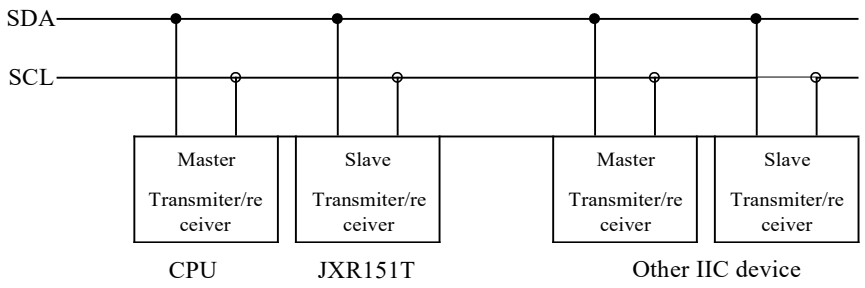


Figure 11-3 IIC system configuration

11.6 Answer signal

The IIC bus has no limit on the number of bytes transferred between the start and end conditions. After each byte of data is transferred, the sender releases the SDA bus and provides an SCL clock to receive the reply signal. If the receiver successfully receives 8 bits of data, the SDA must be set to "0" after the end of the clock for transmitting the last 1bit of data, and the sender will use this low level as the response signal of successful data transmission; After 1 clock cycle, the receiving end releases the SDA bus, ready to receive new data.

The IIC bus terminates the data transfer when the following conditions are met:

(1) When the master device acts as the sender, it sends the termination condition after receiving the reply signal from the slave device.

(2) When the master device acts as the receiver, after successfully receiving 8 bits of data, it sends a "1" as the reply signal and sends the termination condition immediately.

11.7 IIC Bus control

This section describes the IIC bus communication timing for the CPU as the master device and the JXR151T as the slave device.

11.7.1 Write operation with specified address

JXR151T has the address automatic increment function, after setting the operation address, only need to send data continuously, the address bit can be automatically incremented.

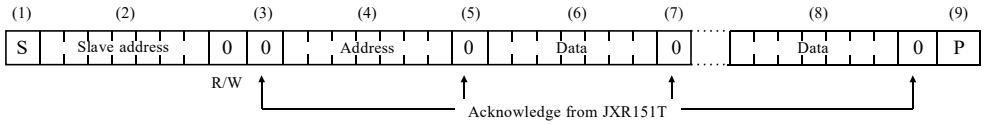


Figure 11-4 Write operation with specified address

(1) CPU send start condition [S].

(2) The CPU sends JXR151T slave address and is set to write mode via R/W bit.

(3) JXR151T produces an answer signal.

(4) The CPU sends the write register address to JXR151T.

(5) JXR151T generates a reply signal.

(6) The CPU sends data to the register corresponding to the address specified in (4).

(7) JXR151T generates a reply signal.

(8) Repeat the process (6) (7), and the address of the write register in JXR151T will automatically increment.

(9) The CPU sends the termination condition [P].

11.7.2 Read operation with specified address

After writing to the register, the CPU can read the register data by setting the read mode.

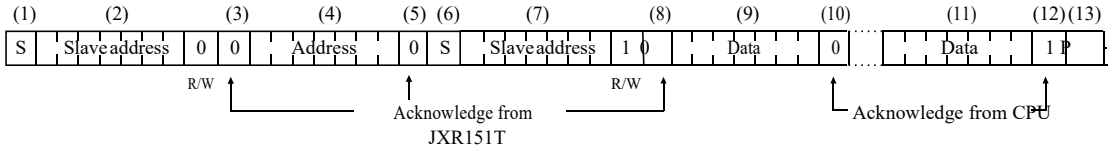


Figure 11-5 Read operation with specified address

(1) The CPU sends the start condition [S].

(2) The CPU sends JXR151T slave address and is set to write mode via R/W bit.

(3) JXR151T produces an answer signal.

(4) The CPU sends the read register address to JXR151T.

(5) JXR151T generates a reply signal.

(6) The CPU resends the start condition.

(7) The CPU sends the JXR151T slave address and is set to read mode via R/W bits.

(8) JXR151T generates a response signal; After that, the CPU acts as the receiver and the JXR151T acts as the transmitter.

(9) JXR151T sends the data in the register corresponding to the address specified in (4).

(10) The CPU sends a reply signal to the JXR151T.

(11) Repeat the process (9) (10) and the address of the read register in JXR151T will automatically increment.

(12) The CPU sends a reply signal to the JXR151T.

(13) The CPU sends the termination condition [P].

11.7.3 Read operation without specified address

The master device goes directly into read mode to read the contents of all registers from the device. If the read operation was performed before the operation, the read operation continues from the read register address +1; If the operation was preceded by a write operation, the read operation starts from the first register address corresponding to the write operation.

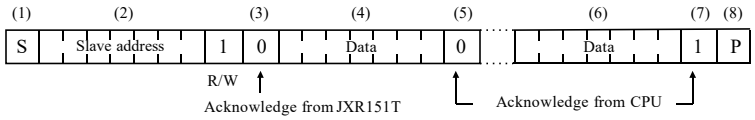


Figure 11-6 Read operation without specified address

(1) CPU send start condition [S].

(2) The CPU sends the JXR151T slave address and is set to read mode via R/W bit.

(3) JXR151T produces a reply signal; After that, the CPU acts as the receiver and the JXR151T acts as the transmitter.

(4) The JXR151T automatically increments the register address and sends the register data.

(5) The CPU sends a reply signal to the JXR151T.

(6) Repeat the process (4) (5) and the address of the read register in JXR151T will automatically increment.

(7) The CPU sends a reply signal to the JXR151T.

(8) CPU send termination condition [P].

Appendix

Application notes

1、The electrostatic protection level of the product is HBM ±4.0kV and CDM ±2.0kV. Electrostatic breakdown should be prevented during using.

2、During the use of the product, power supply glitches exceeding 8.25V may induce the latch - up effect and cause circuit damage. A decoupling capacitor of at least 4.7uF should be added as close as possible to the power pin of the clock chip to ensure the stable operation of the chip.

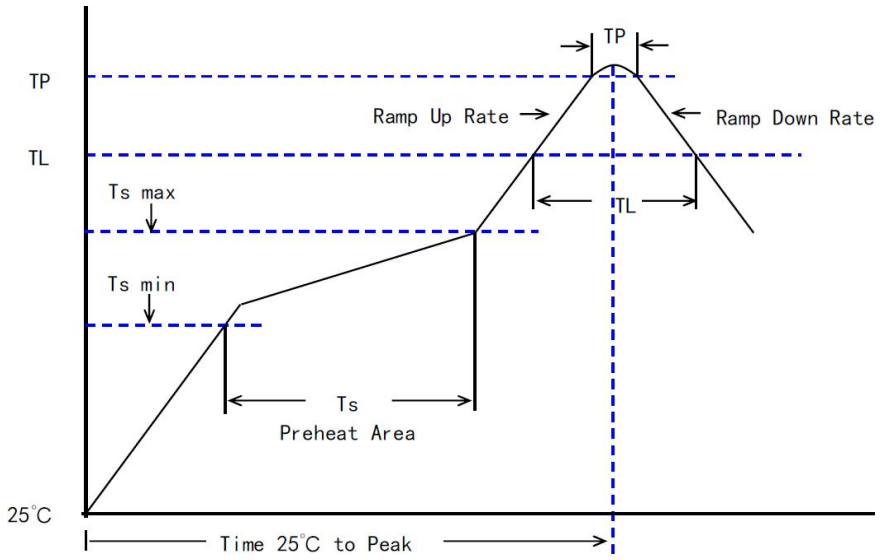
3、Since the clock chip is a low - power integrated circuit product, any high - noise circuit components should be avoided from being placed around the clock chip.

4、The input pins of the chip left floating may lead to an increase in current power consumption. During use, the input pins of the chip should be connected to a fixed potential (VDD or GND).

5、The moisture sensitivity level of the chip is Level 3. Before soldering onto the board after unpacking, the temperature and humidity of the workshop storage environment should not exceed 30℃ and 60%RH respectively, and the storage time should not exceed 168 hours.

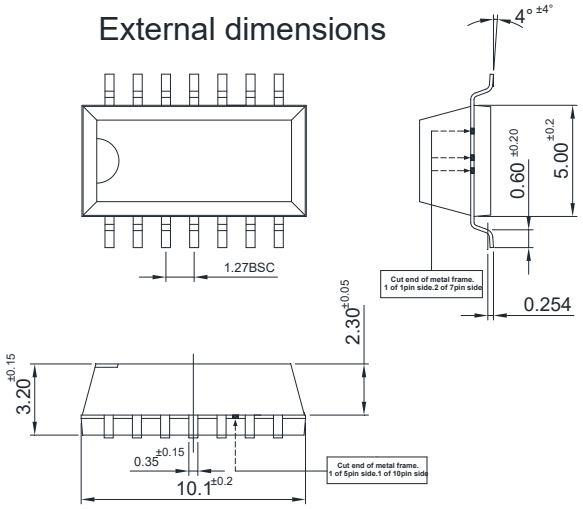
6、During the reflow soldering process, the peak temperature must be strictly controlled not to exceed 260℃. Otherwise, the built - in crystal oscillator may be damaged, resulting in excessive clock deviation or even oscillator stop (recommended reflow curve refers to the figure below).

Profiles Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts Min) Temperature Max (Ts Max) Time (Ts) from (Ts Min to Ts Max)	 150°C 200°C 60 ~ 120 seconds
Ramp-up rate (TL to TP)	3°C/second Max
Liquidous Temperature (TL) Time (TL) maintained above TL	217°C 60 seconds Max
Peak/Classification Temperature (TP)	245±5°C
Time within 5°C of actual Peak Temperature (TP)	10 seconds Max
Ramp-down rate (TP to TL)	6°C/second Max
Time 25°C to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max

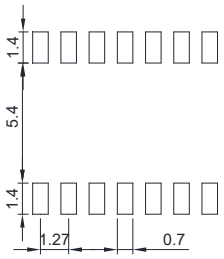

TP
TP
Ramp Up Rate
Ramp Down Rate
TL
Ts max
TL
Ts min
Ts
Preheat Area
25°C
Time 25°C to Peak

Package size

External dimensions



Recommended soldering pattern



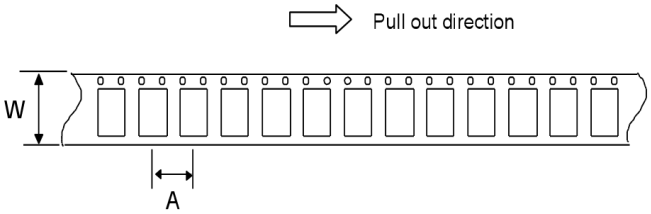
Unit:mm

Packing specifications

SOP Emboss Taping (TE2)

Symbol	SOP14
A	8
W	16

Unit : mm



Symbol	SOP14
A	330
W	16.4

Unit : mm