JXR160 User Manual

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Catalogue

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1 Overview

JXR160 is a real-time clock chip with I²C Bus interface that incorporates a temperature compensated circuit.

JXR160 has a minimal timing unit of 1 second, which can realize automatic leap year correction, and also provides alarm function, fixed-cycle Timer Interupt function, time update interrupt function and 4096Hz/1Hz clock output function.

2 Features

- Built-in temperature compensated circuit, provide high-accuracy clock output between -40~+85 ℃.
- Built-in oscillator load capacitor, with oscillator frequency fine adjustment available.
- Fast I²C Bus Support (@400kHz)
- Multiple interrupt functions including time alarm, fixed-cycle interrupt and time update interrupt.
- Programmable for clock output at 4096Hz/1Hz
- Calendar range 2000-2099 supported, with automatic leap year correction
- Temperature compensation circuit operating voltage range: 2.2V~5V
- I²C Bus operating voltage range: 1.8V~5.5V
- Clock circuit operating voltage range at room temperature: 1.2V~5.5V
- Low current consumption: 2.3μA@3V(Typ)

3 Applications

- Portable devices
- Mobile phones
- Attendance machines
- Smart door locks
- Clocks and calendars

4 Block Diagram

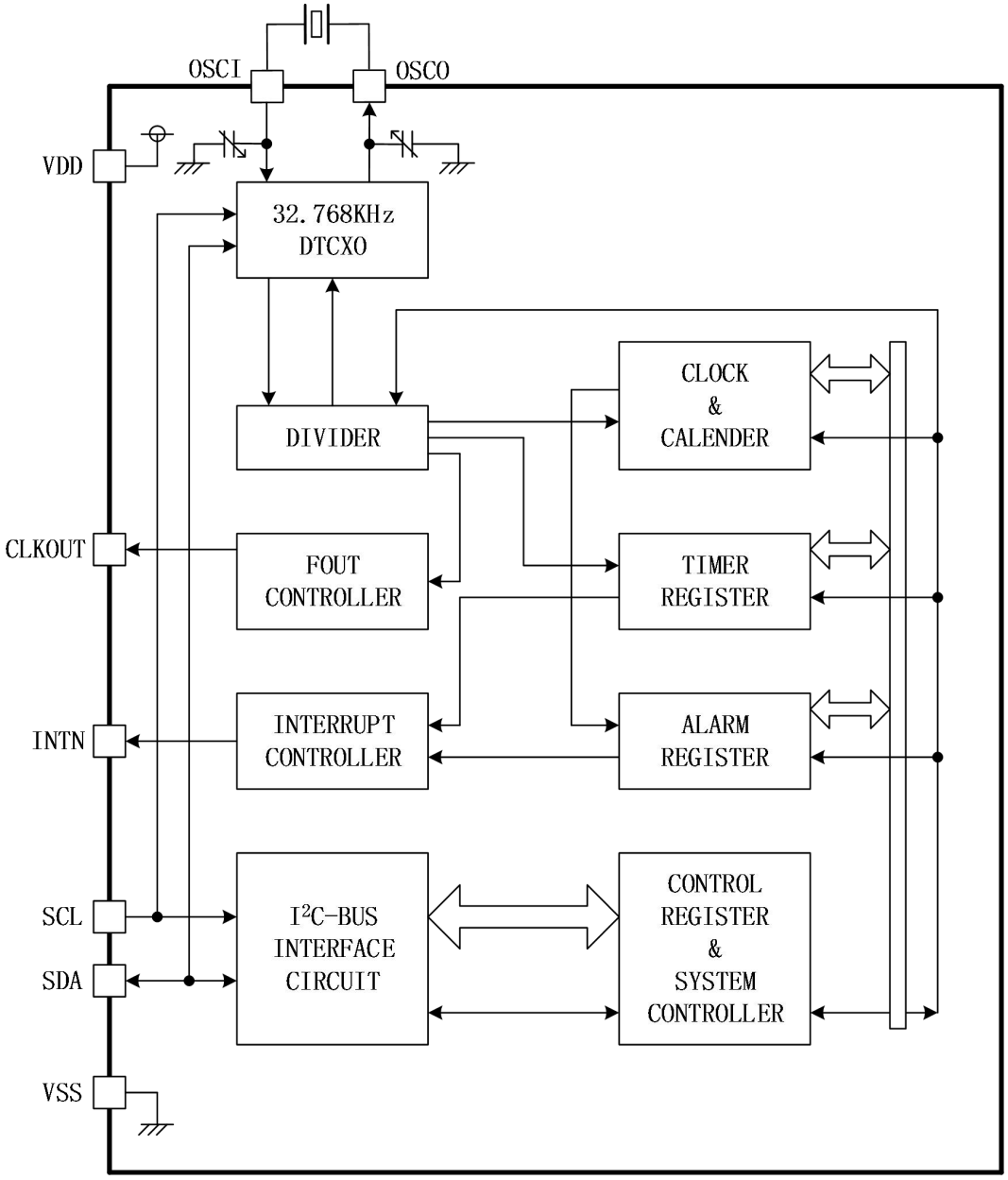


Fig. 4- 1 JXR160 Block Diagram

5 Pin Description

5.1 Package Type

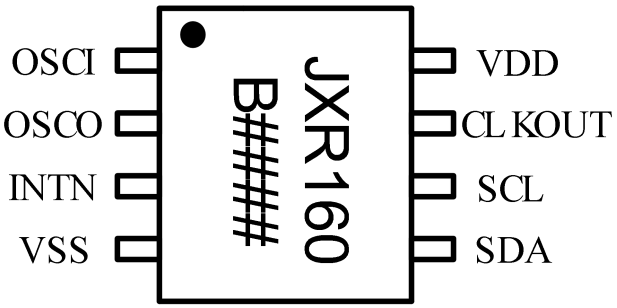


Fig. 5- 1 JXR160 Package Type

5.2 Pin Functions

Table 5- 1 JXR160 Pin Functions

Pin name	I/O	Function
1. OSCI	IN	Oscillator input
2. OSCO	OUT	Oscillator output
3. INTN	OUT	Interrupt output, N-ch open-drain
4. VSS	GROUND	Connect to GND
5. SDA	INOUT	I^2C Bus data transfer terminal
6. SCL	IN	I^2C Bus clock transfer terminal
7. CLKOUT	OUT	Clock output, N-ch open-drain
8. VDD	POWER	Connect to VDD

6 Absolute Maximum Ratings

Table 6- 1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage*1	V_{DD}	Voltage between VDD and VSS	-0.5 to 6	V
Input voltage*1, *2	V_{IN}	SCL, SDA pins	-0.5 to V_{DD}+0.3	V
Output voltage*1, *2	V_{OUT}	CLKOUT, SDA, INTN pins	-0.5 to V_{DD}+0.3	V
Storage temperature	T_{STG}	When stored separately, without packaging	-55 to 150	ºC

*1: All electrical specifications must not exceed the maximum ranges in the table above at any time, as it may cause deterioration of the relevant parameters, reduced reliability or even chip failure.

*2: V_{DD} here refers to the V_{DD} range under operating conditions.

7 Recommended Operating Conditions

Table 7- 1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	Terminal voltage	1.8	3.0	5.5	V
Temperature compensation voltage	V_{TEM}	Temperature compensation circuit operating voltage	2.2	3.0	5.5	V
Clock operating voltage	V_{CLK}	Oscillator module operating voltage	1.2	3.0	5.5	V
Operating temperature	T_{OPR}	---	-40	25	85	ºC

*Any operation that exceeds the recommended range in the table above may seriously affect the chip's reliability.

8 Frequency Characteristics

Table 8- 1 Frequency Characteristics

Item	symbol	Condition	MIN	TYP	MAX	Unit
Frequency stability	Δf/f	Ta=25ºC, V_{DD}=2.2V~5V		±5		$\times10^{-6}$
		Ta=-40 ºC~85 ºC, V_{DD}=2.2V~5V		±20		
Frequency/voltage characteristics	Δf/f/V	Ta=25 ºC, V_{DD}=2.2V~5.5V		±0.5	±1.0	$\times10^{-6}$/V
Oscillation start time	T_{STA}	Ta=25 ºC, V_{DD}=1.8V			0.9	S
		Ta=-40ºC~85 ºC, V_{DD}=1.8V~5.5V			2.0	
Aging	fa	Ta=25 ºC, V_{DD}=3.0V, first year			±1.0	$\times10^{-6}$/year

9 Electrical Characteristics

9.1 DC Characteristics

Table 9- 1 DC Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power consumption	I_{DD1}	CLKOUT = 4096Hz	V_{DD}=5V		2.4	3.2	μA
	I_{DD2}		V_{DD}=3V		2.3	3.0	
High-level input voltage	V_{IH}	SCL, SDA pins		0.7*V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}			0		0.3*V_{DD}	V
Low-level output voltage	V_{OL}	CLKOUT, INTN, SDA pins	I_{OL}=1mA	0		0.3	V
Input leakage current	I_{LK}	SCL, SDA pins, V_{IN}=V_{DD} or GND		-0.3		0.3	μA
Crystal ESR	R_S					70	KΩ
Crystal load capacitance	C_L				12.5		pF
Output leakage current	I_{OZ}	INTN, CLKOUT, SDA, V_{IN}=V_{DD} or GND		-0.3		0.3	μA

9.2 AC Characteristics

Table 9- 2 AC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	---			400	KHz
Start condition setup time	$t_{SU;STA}$	---	0.6			μS
Start condition hold time	$t_{HD;STA}$	---	0.6			μS
Data setup time	$t_{SU;DAT}$	---	100			nS
Data hold time	$t_{HD;DAT}$	---	0		700	nS
Stop condition setup time	$t_{SU;STO}$	---	0.6			μS
Bus idle time	t_{BUF}	Between start condition and stop condition	1.3			μS
Time when SCL = 'L'	t_{LOW}	---	1			μS
Time when SCL = 'H'	t_{HIGH}	---	1			μS
Rise time for SCL and SDA	t_r	---			0.3	μS
Fall time for SCL and SDA	t_f	---			0.3	μS
Allowable spike time on bus	t_{SP}	---			50	nS
Frequency output duty cycle	Duty	Calculated with output reaches 50% of V_{DD}	40	50	60	%

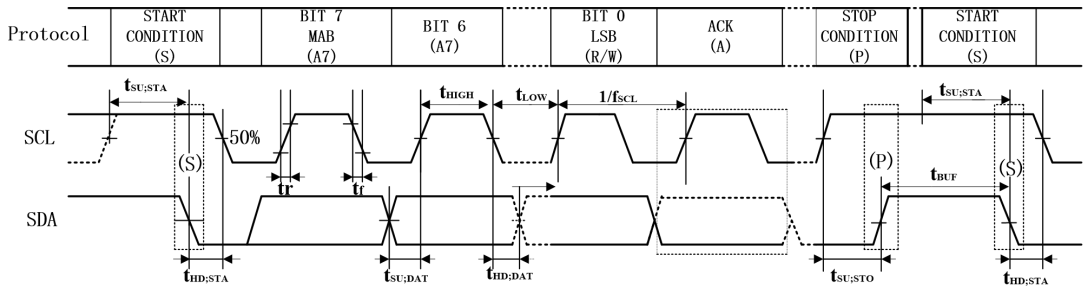


Fig. 9- 1 I²C Timing Diagram

*When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds. If such time limit is exceeded, the I²C Bus interface is reset by the internal timer.

10 Registers

10.1 Register Table

Table 10- 1 Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	SEC	○	40	20	10	8	4	2	1
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1
03	WEEK	○	6	5	4	3	2	1	0
04	DAY	○	○	20	10	8	4	2	1
05	MONTH	○	○	○	10	8	4	2	1
06	YEAR	80	40	20	10	8	4	2	1
07	RAM	•	•	•	•	•	•	•	•
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0B	Timer Counter 0	128	64	32	16	8	4	2	1
0C	Timer Counter 1	•	•	•	•	2048	1024	512	256
0D	Extension Register	○	WADA	USEL	TE	•	•	TSEL1	TSEL0
0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET
0F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET
20	OSC Offset Ctrl	○	○	○	○	OFS3	OFS2	OFS1	OFS0

*Ensure that valid values are written to the Calendar and clock register, otherwise the chip will not be able to operate properly.

*The register bit marked with '○" is read only, with a read value of '0'. The register bit marked with '•" can be used as RAM to perform read and write operations.

*If the alarm interrupt function is not set (AIE = '0'), register 08~0A can be used as RAM.

*If the timed interrupt function is not set (TE = TIE = '0'), register 0B and 0C can be used as RAM.

*UF, TF, AF, VLF and VDET bits are only allowed to be written to '0'.

*When the chip is powered up, CSEL0 is preset to '1', CSEL1, VLF, UIE, TIE, AIE bits are preset to '0'.

10.2 Register Description

10.2.1 Clock and Calendar Register(Register 00 to 06)

- Data Format

The data is in BCD code except for WEEK register (Register 13). For example, the value '01011001' in the SECOND register means that the current time is 59 seconds.

The timing system is fixed to 24-hour system.

- YEAR register and leap years

The time range of the YEAR register is 00 - 99. After 99, it overflows back to 00. If the value represented by the YEAR register is divisible by 4, this year is recognized as a leap year. The valid time range of the calendar is 2000~2099.

- WEEK register

The day (of the week) is indicated by 7 bits, which is bit 0 to bit 6. Each valid bit represents a day from Monday to Sunday. Therefore only one bit of this register is allowed to be '1'.

Table 10- 2 WEEK Register

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Day
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

10.2.2 Alarm Registers(Register 08 to 0A)

The alarm time can be set to the minute of the day every week or the minute of the day every month. (WEEK alarm mode or DAY alarm mode), and this mode can be adjusted by writing the WADA bit of register 0D.

Each alarm register has AE (Alarm Enable) bit (bit7). When the AE bit of a certain alarm register is '0', the set value of this register needs to be compared with the corresponding timing register, and an alarm interrupt is output when the value is the same. If AE bit is '1', the alarm register is always considered the same as the corresponding register.

When WEEK alarm mode is selected, several days of the week can be selected at the same time, i.e., several bits in the WEEK alarm function in register 0A (bit0 ~bit6) can be set to '1' at the same time. The correspondence in WEEK alarm mode can be referred to in Table 10-3.

Table 10- 3 WEEK Alarm Mode Register 0A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0A	WEEK Alarm	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

10.2.3 Fixed-Cycle Counter Control Register(Register 0B, 0C)

These two registers are used to set the preset countdown value for fixed-cycle interrupts. When

the values of these two registers change from 0001H to 0000H, the fixed-cycle interrupt event occurs. Then TF is set to '1' and INTN outputs 'L' (If TIE is '1'). After that, register 0B and 0C are reset to preset value, and restart the countdown process.

10.2.4 Control Registers and Flag Registers (Register 0D to 0F)

- WADA bit

Used to select alarm interrupt mode. When this bit is set to '1', it is DAY Alarm Mode. When it is set to '0', it is WEEK Alarm Mode.

- USEL bit

Used to set the period of time update interrupt. USEL bit is uncertain when chip is powered up, and needs to be configured manually.

Table 10- 4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

When this bit is set to '1', the down counter for fixed-cycle timer starts counting down and stops when it is set to '0'.

- TSEL bit

Used to set the count period for fixed-cycle interrupts.

Table 10- 5 Fixed-cycle Interrupt Counting Period Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF bits

AF -- alarm interrupt flag, TF -- fixed-cycle interrupt flag, UF -- time update interrupt flag.When the interrupt event occurs, the corresponding flag bit is set to '1'. The flag bit will remain at '1' until it is manually cleared. It is prohibited to manually set these flag bits to '1'.

- AIE，TIE，UIE bits

These three flag bits are used to set the interrupt signal output on the INTN pin when an alarm interrupt, time update interrupt or fixed-cycle interrupt or event occurs. When chips is powered up, these three flag bits are set to '0' by default.

The interrupt signal outputs on the INTN pin is the logic OR of (time update interrupt | fixed-cycle interrupt | alarm interrupt), and the interrupt flag bits are used to determine the specific interrupt outputs.

- VLF bit

Low power supply voltage detection flag. When the power supply voltage is detected to drop below 1.8V, causing the circuit to possibly not operate properly, this bit is set to '1'. This bit will remain at '1' until it is manually cleared. It is prohibited to manually set these flag bits to '1'.

- VDET bit

Voltage detection flag bit. When the power supply voltage is detected to drop below 2.2V, causing the temperature compensation circuit not to operate properly, this bit is set to '1'. This bit will remain at '1' until it is manually cleared. It is prohibited to manually set these flag bits to '1'.

- CSEL bit

Used to set the interval that the temperature compensation circuit operates. CSEL is set to '01' by default (which means 2 seconds), when chip is powered up.

Table 10- 6 Temperature Compensation Operation Interval Selection

CSEL1	CSEL0	Operation interval
0	0	0.5S
0	1	2S *Default
1	0	10S
1	1	30S

- RESET bit

When RESET bit is set to '1', registers of seconds or less are reset, and the clock stops. Meanwhile, temperature compensation and VLF/VDET Voltage detection is disabled.

In the following cases, the RESET bit that is already set to '1' will be cleared:

a) I^2C stop condition detected

b) I^2C restart condition detected

c) I^2C reset detected

At the same time, VLF/VDET will be cleared, the power supply voltage detection function is reset.

10.2.5 OSC Offset Control Register (Register 20)

Table 10- 7 OSC Offset Control Register

Register	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
20	OSC Offset Ctrl	○	○	○	○	OFS3	OFS2	OFS1	OFS0

This register is used to adjust the frequency of the oscillator. Please check the value carefully before adjusting, and the specific adjustment methods are as follows.

Table 10- 8 Output Frequency Adjustment

OFS3	OFS2	OFS1	OFS0	Adjustment value（ppm）
0	0	0	0	0
0	0	0	1	-0.35
0	0	1	0	-0.7
0	0	1	1	-1.05
0	1	0	0	-1.4
0	1	0	1	-1.75
0	1	1	0	-2.1
0	1	1	1	-2.45
1	0	0	0	2.8
1	0	0	1	2.45
1	0	1	0	2.1
1	0	1	1	1.75
1	1	0	0	1.4
1	1	0	1	1.05
1	1	1	0	0.7
1	1	1	1	0.35

11 Interrupt Functions

11.1 Alarm Interrupt

Alarm interrupts can be generated on set days, weeks, hours or minutes.

11.1.1 Alarm Interrupt Timing

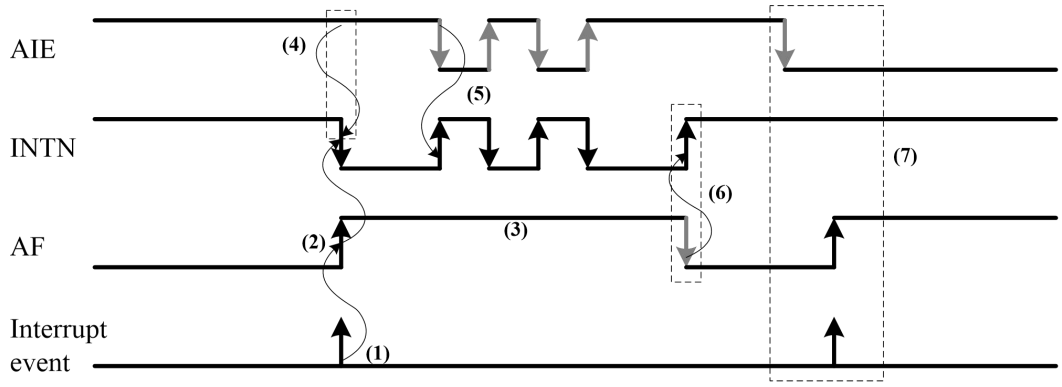


Fig. 11- 1 Alarm Interrupt Timing

(1) Set the hour, minute, date or day of the week information corresponding to the alarm interrupt and the WADA register, and an alarm interrupt event will be generated when the set time matches the current time.

(2) When the alarm interrupt event is generated, AF flag is set to '1'.

(3) AF register will maintain '1' until it is manually cleared.

(4) When alarm interrupt event occurs, if AIE = '1', INTN outputs 'L', if AIE '0', INTN is held in a high resistance state.

(5) If AIE is set to '0' during INTN = '0', INTN instantly returns to the high resistance state. AIE can be used to control the output state of INTN until an alarm interrupt event occurs and the AF register is cleared.

(6) The alarm output can be cleared by clearing AF register, and INTN instantly change to high resistance state from '0'.

(7) If AIE = '0' when alarm interrupt event occurs, INTN maintains high resistance state and will not output 'L'.

11.1.2 Alarm Interrupt Related Registers

Table 11- 1 Alarm Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D or 1D	Extension Register	○	**WADA**	USEL	TE	•	•	TSEL1	TSEL0
0E or 1E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

- It is recommended to set AIE to '0' first when configuring alarm interrupt register in case unwanted hardware interrupt is generated.
- WADA is used to select alarm interrupt mode. When this bit is set to '1', it is DAY Alarm Mode. When it is set to '0', it is WEEK Alarm Mode.
- The occurrence of an alarm interrupt event sets the AF flag to '1', and this bit will maintain '1' until it is cleared manually.
- When an alarm interrupt event occurs, AIE decides whether or not to generate an interrupt signal output. (If AIE = '1', then INTN = '0'. If AIE = '0', then INTN = Hi-Z).
- When the AE bit is '0', the set value of this register needs to be compared with the corresponding timing register. If AE = '1', the register will not be compared, in other words, we consider that this register always matches the corresponding CLOCK or CALENDAR register. Refer to following example:

  (1) When register 0A is set to 0x80, only MINUTE Alarm and HOUR Alarm register need to be compared with corresponding clock registers, the WEEK/DAY register is ignored. Therefore, as long as the HOUR register and the MINUTE register match, alarm interrupt events will be generated every day.

  (2) Setting 1 to the AE bit in each of the three registers (08,09,0A) will cause an alarm interrupt to be generated every minute.

11.2 Fixed-Cycle Interrupt

The fixed-cycle interrupt can generate interrupt alarm events between 244.14μs and 4095 minutes on a fixed cycle.

11.2.1 Fixed-Cycle Interrupt Timing

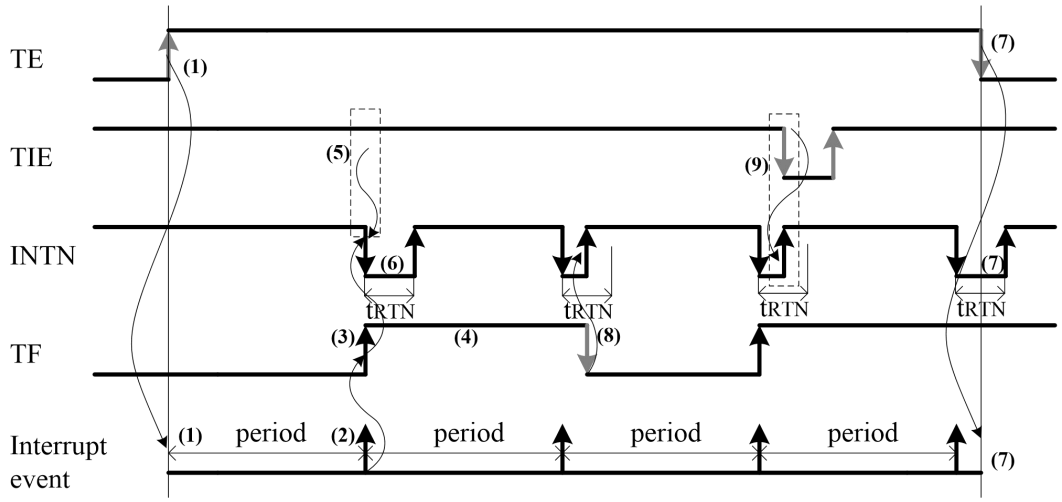


Fig. 11- 2 Fixed-Cycle Interrupt Timing

(1) When TE bit is set to '1', the fixed-cycle counter start to countdown from the preset value.

(2) An interrupt event is generated hen the fixed-cycle counter counts from 0001H to 0000H. The counter is reset to preset value, and starts the next countdown.

(3) When the fixed-cycle interrupt event occurs, TF register is set to '1'.

(4) TF register will maintain '1' until it is cleared manually.

(5) When the fixed-cycle interrupt event occurs, if TIE = '1', INTN outputs 'L'. If TIE = '0', INTN maintains 'Hi-Z'.

(6) INTN outputs a low level voltage ('L') for the length of tRTN, after which it will automatically return to 'Hi-Z' until the next interrupt signal is output.

(7) When TE bit is set to '0', the fixed-cycle counter stops and INTN outputs 'Hi-Z'. (If TE is set to '0' during INTN = '0', INTN recovers to 'Hi-Z' after tRTN).

(8) If TF is cleared during INTN = '0', INTN will recover to 'Hi-Z' immediately.

(9) INTN recovers to 'Hi-Z' instantly when TIE is set to '0'. If TIE is set to '1' again during tRTN, INTN maintains 'Hi-Z'.

11.2.2 Fixed-Cycle Interrupt Related Registers

Table 11- 2 Fixed-Cycle Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C or 1C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D or 1D	Extension Register	○	WADA	USEL	**TE**	•	•	**TSEL1**	**TSEL0**
0E or 1E	Flag Register	○	○	UF	**TF**	AF	○	VLF	VDET
0F or 1F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	○	○	RESET

- It is recommended to set TE and TIE to '0' before configuring the fixed-cycle interrupt register in case unwanted hardware interrupt is generated during the operation.
- TSEL1 and TSEL0 are used to set the period of fixed-cycle interrupt. The automatic reset time of the interrupt signal on the INTN pin is related to the countdown period.

Table 11- 3 Fixed-Cycle Interrupt Period and Its Auto Reset Time

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122mS
0	1	64Hz	7.8125mS
1	0	1Hz	7.8125mS
1	1	1/60Hz	7.8125mS

- Register 0B or 1B, 0C or 1C are used to set the default value of the counter (0001H~FFFFH), the counter generates a fixed-cycle interrupt event when it counts down to 0000H with the counting period set by TSEL.
- TE is the enable control bit of the fixed-cycle counter. When TE = '1', the counter starts. When TE = '0', the counter stops and the fixed-cycle interrupt function is disabled.
- TF is set to '1' when the fixed-cycle interrupt event occurs and it will maintain '1' until it is cleared manually.
- TIE decides whether to generate an interrupt signal output when a fixed-cycle interrupt event occurs (If TIE = '1', INTN = '0'. If TIE = '0', INTN = 'Hi-Z').

Table 11- 4 Fixed-Cycle Interrupt Period

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μS	15.625mS	1S	1min
……	……	……	……	……
2048	500mS	32S	2048S	2048min
……	……	……	……	……
4095	0.9998S	63.984S	4095S	4095min

11.2.3 Generate 4096Hz Square Wave by Pin Multiplexing Fixed-cycle Interrupt Function on CLKOUT Pin

It is available to generate a 4096Hz square wave on CLKOUT pin by configuring specific fixed-cycle interrupt function. And the steps are as follows..

- Set TSEL1, TSEL0, TIE, UIE, AIE to 1'b0 (1 bit binary code '0')
- Set Register 0B to 8'h01, Register 0C to 8'h00
- Set Register TE to 1'b1
- Set Register TIE to 1'b1

11.3 Time Update Interrupt

Depending on the set value, the time update interrupt generates time update interrupt in seconds or minutes.

11.3.1 Time Update Interrupt Timing

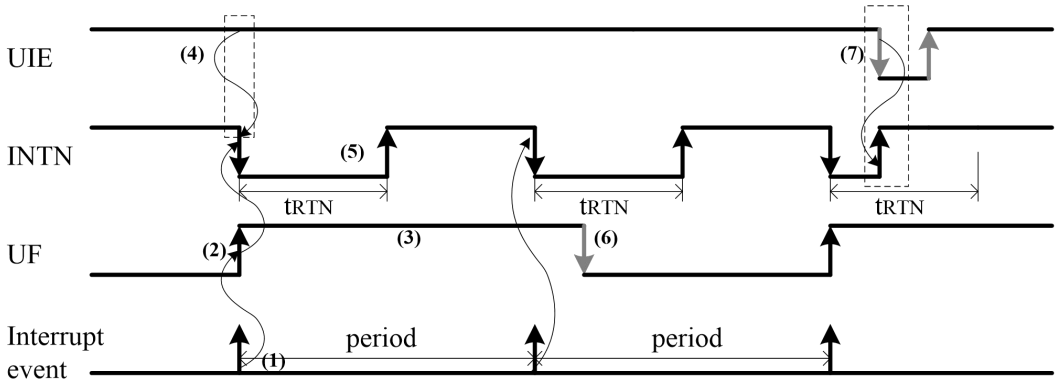


Fig. 11- 3 Time Update Interrupt Timing

(1) USEL register determines whether the chip is in a SECOND or MINUTE update mode. When the corresponding SECOND or MINUTE register updates, time update interrupt is generated.

(2) UF register is set to '1' when time update interrupt occurs.

(3) UF register will maintain '1' until it is manually cleared.

(4) When time update interrupt occurs, if UIE = '1', INTN outputs 'L'. If UIE = '0', INTN maintains 'Hi-Z'.

(5) INTN outputs a low level voltage ('L') for the length of tRTN, after which it will automatically return to 'Hi-Z' until the next interrupt signal is output.

(6) If UF is cleared (set to '0') during INTN = '0', INTN will recover to 'Hi-Z' after tRTN.

(7) IF UIE is set to '0' during INTN = '0', INTN recovers to 'Hi-Z' instantly and interrupt signal output stops. If UIE is set to '1' during tRTN again, INTN will maintain 'Hi-Z'.

11.3.2 Time Update Interrupt Related Registers

Table 11- 5 Time Update Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension Register	○	WADA	**USEL**	TE	•	•	TSEL1	TSEL0
0E or 1E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
0F or 1F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

- It is recommended to set UIE to '0' before configuring time update interrupt register in case unwanted hardware interrupt is generated during the operation.
- USEL signal is used to set whether the interrupt mode is SECOND update or MINUTE update.

Table 11- 6 Time Update Interrupt Mode Control

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of time update interrupt event will set UF to '1' and it maintains '1' until it is manually cleared.
- UIE determines whether or not to generate an interrupt signal output. (If UIE = '1', INTN = '0'. If UIE = '0', INTN = 'Hi-Z').

11.3.3 Generate 1Hz Square Wave by Pin Multiplexing Time Update Interrupt Function on CLKOUT Pin

It is available to generate 1Hz square wave by configuring time update interrupt function, and the specific steps are as follows.

- Set USEL, TIE, AIE to 1'b0
- Set UIE to 1'b1

12 I²CBus Interface

12.1 Characteristics of I²C Bus Interface

The I²C bus supports bi-directional communications, and its signal line SDA as well as the clock line SCL need to be connected to a high level voltage through a pull-up resistor. The port connected to the I²C bus must be open-drain in order to realize multi-device wired-AND logic connections.

12.2 Data Transfers

One bit of data can be transmitted per SCL clock cycle. When sending data, the data on the SDA line changes during SCL is 'L'. When receiving data, valid data can be obtained from the data line SDA during SCL is 'H'.

12.3 Starting and Stopping Conditions

In the idle state, both SCL and SDA are held high. During SCL is 'H', the falling edge of SDA is used as the start condition for I²C communication, and the rising edge of SDA is used as the stop condition for I²C communication.

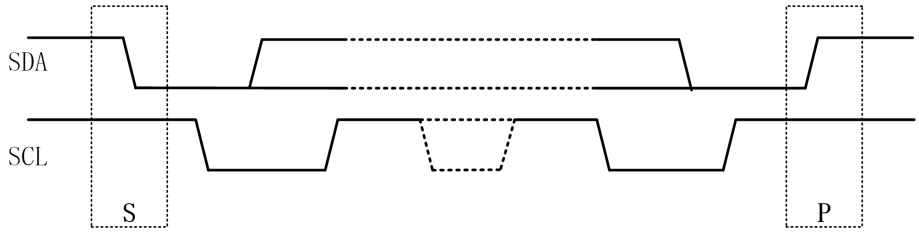


Fig. 12- 1 I²C Starting and Stopping Conditions

12.4 Device Selection (Slave Address)

The I²C Bus devices do not have any chip select or chip enable pins. The chip selection on the I²C BUS is executed when the interface starts. The master device send the required slave address to all devices on the I²C Bus. The slave device sends a acknowledge signal to setup communication with master device.

Slave address includes 7 bits of data ,4 bits (Group 1) + 3 bits(Group 2). The slave address of JXR160 is '0110010". During the communication process, the slave address and R/W bit is sent as 8bit data.

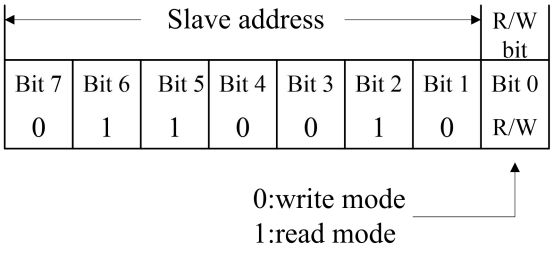


Fig. 12- 2 I²C Slave Address

12.5 System Configuration

The device that will control the data transfer becomes the mater device and the devices that are controlled by the master device become the slave devices. The device that sends data is called the transmitter and the device that receives data is called the receiver.

In the JXR160 system, CPU or other controlling device become the master device and JXR160 itself becomes slave device. Both master and slave device can become transmitter or receiver.

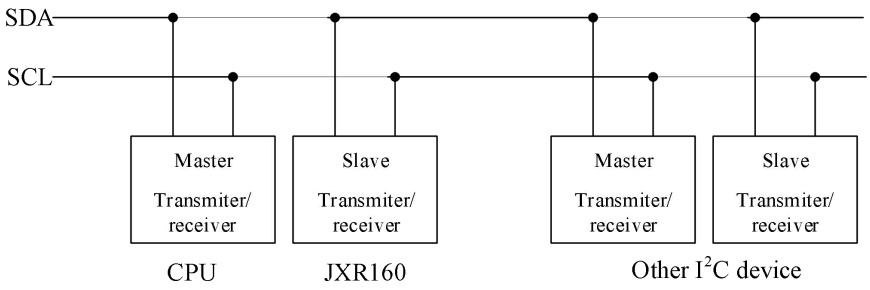


Fig. 12- 3 I²CSystem Configuration

12.6 Acknowledge Signal

The I²C-bus has no limit on the number of bytes that can be transferred between the start and stop conditions. After each byte of data has been transferred, the transmitter releases the SDA bus and provides and SCL clock to receive an answer signal. If the receiver receives 8bit data successfully, it needs to set SDA to 0 after the end of the clock of transmitting the last 1bit data, and the transmitter will consider this low level voltage as the answer signal for successful data transmission. After 1 clock cycle, the receiver releases the SDA bus and is ready to receive new data.

The I²C-bus terminates data transfer when the following conditions are met:

(1) When the master device acts as the transmitter, it sends the termination condition after receiving the answer signal from the slave device.

(2) When the master device acts as the receiver, it sends '1' as a acknowledge signal and then send a stop condition after receiving 8bit data successfully.

12.7 I²C-Bus Control

In the following sequence descriptions, it is assumed that the CPU is the master and the JXR160 is the slave.

12.7.1 Address Specification Write Operation

Since the JXR160 has address auto increment function, once the initial address has been specified, the JXR160 increments the receive address each time data is transferred automatically.

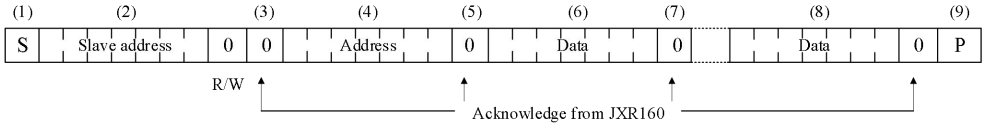


Fig. 12- 4 Address Specification Write Operation

(1) CPU transfers start condition [S].

(2) CPU transfers the JXR160's slave address with the R/W bit set to write mode.

(3) JXR160 generates acknowledge signal.

(4) CPU transmits write address to JXR160.

(5) JXR160 generates acknowledge signal.

(6) CPU transfers write data to the address specified at (4) above.

(7) JXR160 generates acknowledge signal.

(8) Repeat (6) and (7) if necessary. Write addresses in JXR160 will increase automatically.

(9) CPU transfers stop condition [P].

12.7.2 Address Specification Read Operation

After writing to the register, CPU can read the register by setting read mode.

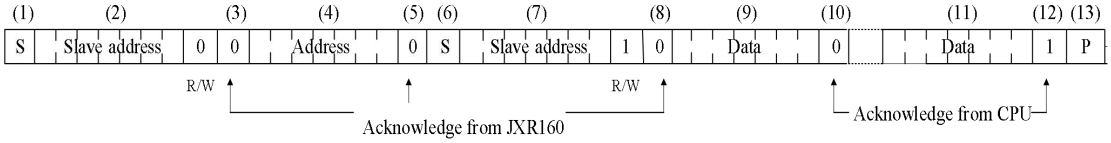


Fig. 12- 5 Address Specification Read Operation

(1) CPU transfers start condition [S].

(2) CPU transfers the JXR160's slave address with the R/W bit set to write mode.

(3) JXR160 generates acknowledge signal.

(4) CPU transmits read address to JXR160.

(5) JXR160 generates acknowledge signal.

(6) CPU transfers start condition [S].

(7) CPU transfers the JXR160's slave address with the R/W bit set to read mode.

(8) JXR160 generates acknowledge signal, then CPU acts as receiver and JXR160 acts as a transmitter.

(9) Data from address specified at (4) above is output by JXR160.

(10) CPU generates acknowledge signal.

(11) Repeat (9) and (10) if necessary. Read addresses in JXR160 will increase automatically.

(12) CPU generates acknowledge signal.

(13) CPU transfers stop condition [P].

12.7.3 Read Operation When Address Is Not Specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address +1.

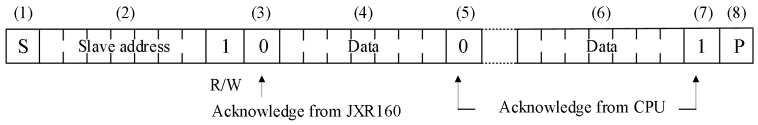


Fig. 12- 6 Read Operation When Address Is Not Specified

(1) CPU transfers start condition [S].

(2) CPU transfers the JXR160's slave address with the R/W bit set to read mode.

(3) JXR160 generates acknowledge signal, then CPU acts as receiver and JXR160 acts as a transmitter.

(4) JXR160 increase the read address automatically and transmit the data in the register.

(5) CPU generates acknowledge signal.

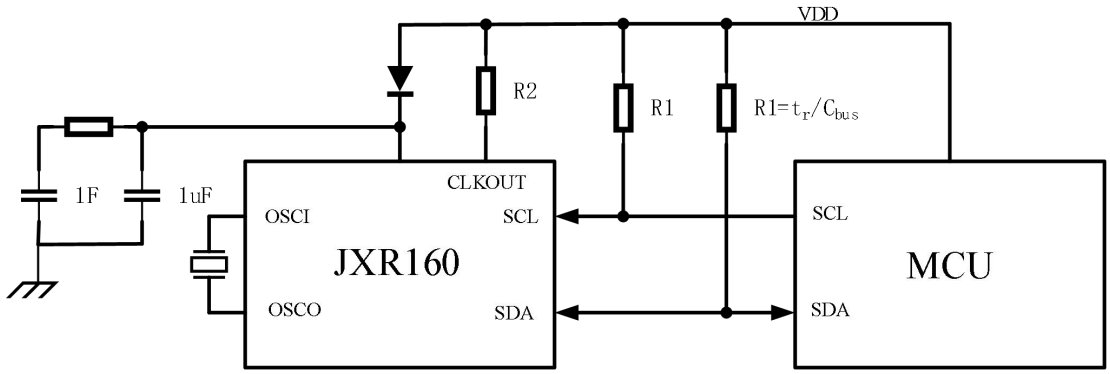
(6) Repeat (4) and (5) if necessary. Read addresses in JXR160 will increase automatically.

(7) CPU generates acknowledge signal.

(8) CPU transfers stop condition [P].

Appendix

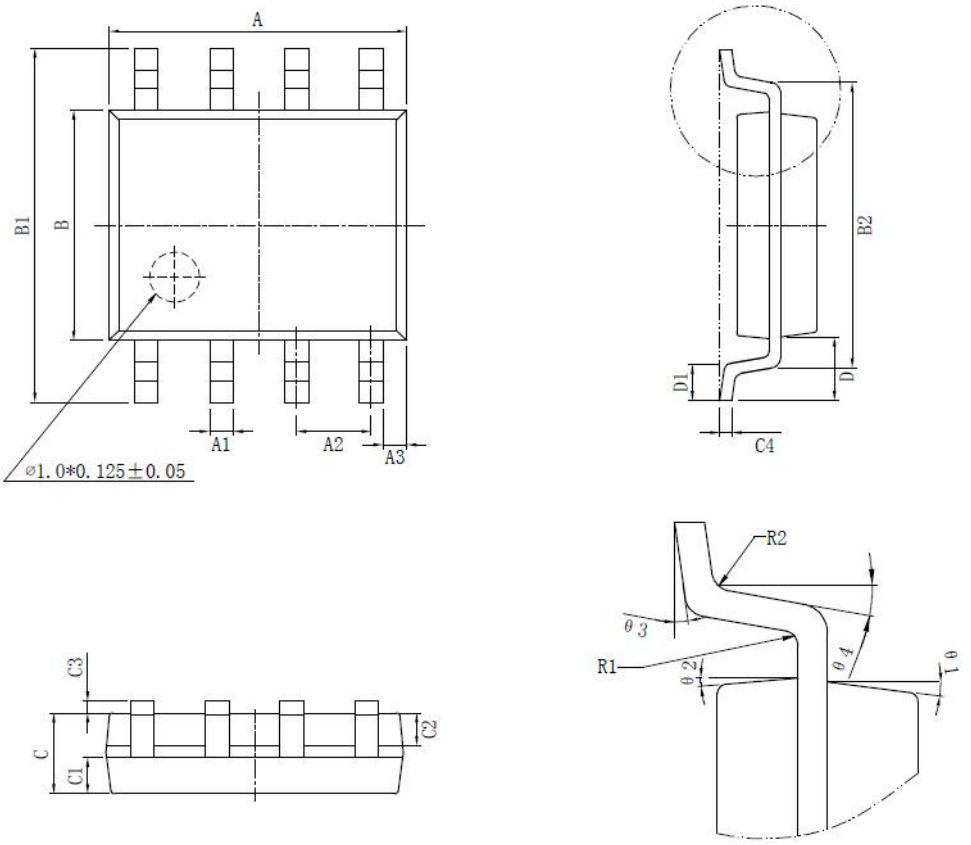
Example of Applications



- The pull-up resistor for the I2C-Bus is determined by the communication speed. Based on empirical data, a communication rate of 100kHz is guaranteed when R1 is 10KΩ, and a communication rate of 400kHz is guaranteed when R1 is 4.7KΩ.
- CLKOUT is an N-ch open-drain structure, and a pull-up resistor R2 is needed when measuring frequency output.
- In order to avoid unnecessary power fluctuations that affects the performance of the chip, a decoupling capacitor of 1uF should be added at the power pin (PIN8) of the chip.

Package Size

Symbol Size	Min.(mm)	Max(mm)	Symbol Size	Min.(mm)	Max(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17°TYP4	
C	1.30	1.60	θ2	13°TYP4	
C1	0.55	0.65	θ3	0°~8°	
C2	0.55	0.65	θ4	4°~12°	

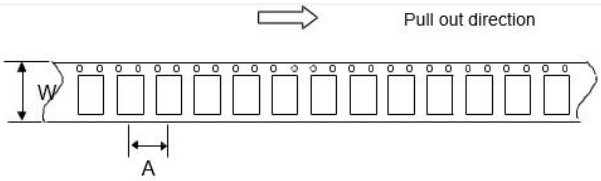


Packaging Specifications

SOP Emboss Taping (TE2)

Symbol	SOP8
A	8
W	12

Unit : mm



Symbol	SOP8
A	330
W	12.4
Contents	4000 pcs

Unit : mm