JXR191T(LP)-GA User Manual

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catalogue

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1 summary

The JXR191T (LP)-GA is a high-precision real-time clock chip with an IIC interface and an integrated 32.768kHz temperature-compensated crystal oscillator (D-TCXO). It features a minimum timing unit of milliseconds, automatic leap year correction, and provides interrupt outputs for timing alarms, fixed-period interrupts, and time updates. Additionally, it offers clock outputs at 32.768kHz, 1024Hz, 32Hz, and 1Hz.

The chip has obtained AEC-Q100 automotive-grade certification, with a temperature range of-45℃ to 125℃. It delivers ultra-precise clock signals within-45℃ to 105℃ and provides temperature output with absolute accuracy of ±1℃. The chip features automatic standby power switching, automatically switching to backup power when the main power supply fails.

2 characteristic

- Built-in high-precision 32.768kHz D-TCXO
- ms precision
- Supports high-speed IIC bus protocol (400kHz)
- The operating temperature range covers-45℃ to 125℃.
- High Frequency Stability (UA):
- 25°C: <1.0 ppm; (daily timing error less than 0.086 s)
- 0°C to 50°C: <1.5 ppm; (daily timing error less than 0.130 s)
- -45°C to 85°C: <3.0 ppm; (daily timing error less than 0.259 s)
- 85°C to 105°C: <5.0 ppm; (daily timing error less than 0.432 s)
- Time alarm interrupt function (settable: day, week, hour, minute)
- Fixed cycle interrupt function
- Time update interrupt function
- Clock output with enable control at 32.768kHz/1024Hz/32Hz/1Hz
- The calendar range supports years from 2000 to 2099 and automatically adjusts for leap years.
- The operating voltage range of the temperature compensation circuit is 1.8V to 5.5V.
- The clock circuit operates within a voltage range of 1.0V to 5.5V.
- Built-in 64-byte user RAM
- Low current power consumption: 0.9μA@3V (Typ)
- Certified to AEC-Q100 automotive-grade standards

3 structured flowchart

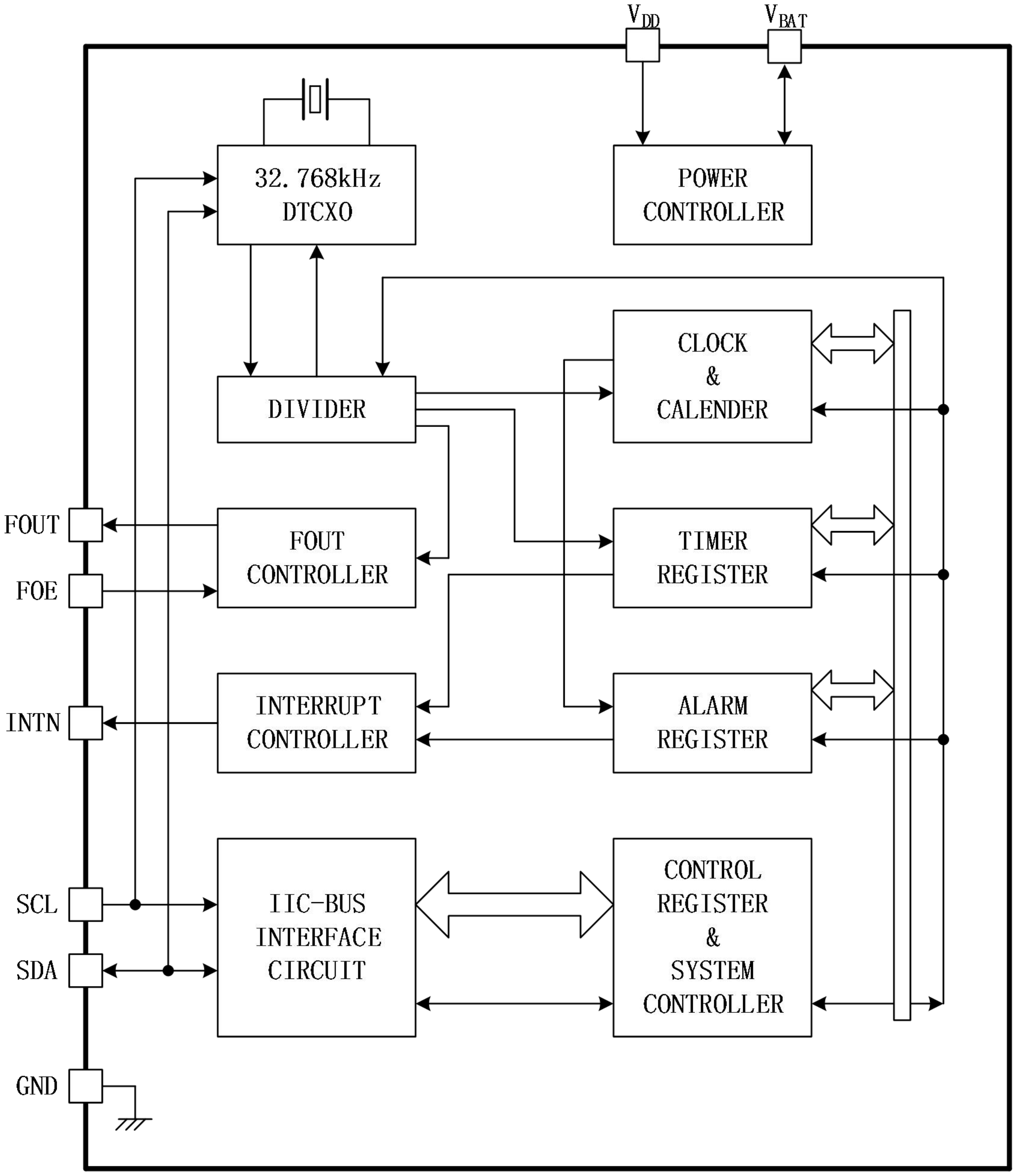


Figure 3-1 Block diagram of the JXR191T (LP)-GA system

4 Pin definition

4.1 Package form

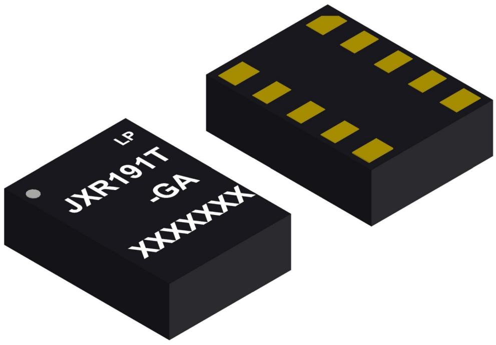


Figure 4-1 JXR191T (LP)-GA package form

4.2 Pin functions

Table 4-1 JXR191T (LP)-GA Pin Definitions

Pin name	I/O	Function
1. FOE	INPUT	FOUT output enable. When FOE = '1', FOUT provides frequency output. The chip defaults to pull-down mode.
2. V_{DD}	POWER	main power source
3. V_{BAT}	POWER	Backup power supply; if the automatic switching function for backup power is not required, this pin must be shorted to V_{DD}
4. FOUT	OUTPUT	The 32.768kHz frequency output port is controlled by FOE. When FOE is '1', it outputs a 32.768kHz clock signal; when FOE is '0', it outputs a high-impedance state.
5. SCL	INPUT	IIC bus communication serial clock input
6. NC	------	No connection required. Keep it suspended.
7. SDA	INOUT	IIC bus communication data transmission end, N-channel open drain output
8. NC	------	No connection required. Keep it suspended.
9. GND	GROUND	power supply ground terminal
10. INTN	OUTPUT	Interrupt output port, N-channel open drain output

5 absolute maximum rating

Table 5-1 Absolute Maximum Rated Value

Item	Symbol	Condition	Rating	Unit
Power Supply Voltage*1	V_{DD}	Voltage between V_{DD} and GND	-0.5 to 6	V
Input voltage *1, *2	V_{IN}	FOE, SCL, SDA pins	-0.5 to V_{DD} + 0.5	V
Output voltage*1, *2	V_{OUT}	FOUT, SDA, INTN pins	-0.5 to V_{DD} + 0.5	V
storage temperature	T_{STG}	Dispersed storage, unpackaged	-55 to 125	℃

*1: All electrical parameters must never exceed the maximum rated values specified in the table. Exceeding these limits may degrade performance, reduce reliability, or even cause chip failure.

*2: V_{DD} denotes the recommended operating voltage range.

6 Recommended operating conditions

Table 6-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
control voltage	V_{DD}	interface voltage	1.2	3.0	5.5	V
temperature compensation voltage	V_{TEM}	working voltage of temperature compensation circuit	1.8	3.0	5.5	V
clock operating voltage	V_{CLK}	operating voltage of oscillator module	1.0	3.0	5.5	V
temperature compensation range	V_{COMP}	Temperature range of compensation	-45	25	105	℃
service temperature	T_{OPR}	---	-45	25	125	℃

Any operation beyond the recommended range in the table may significantly compromise the chip's reliability.

7 frequency characteristic

Table 7-1 Frequency Characteristics

Item	symbol	Condition		MIN	MAX	Unit
frequency stability	Δf/f	Ta = 25°C, V_{DD} = 3.0V	UA/UB/UC	-1.0	+1.0	×10^{-6}
			UD	-5.0	+5.0	
		Ta = 0°C ~ 50°C, V_{DD} = 3.0V	UA	-1.5	+1.5	
			UB	-3.0	+3.0	
			UC	-3.8	+3.8	
		Ta = -30°C ~ 70°C, V_{DD} = 3.0V	UC	-5.0	+5.0	
		Ta = -45°C ~ 85°C, V_{DD} = 3.0V	UA	-3.0	+3.0	
			UB	-5.0	+5.0	
			UC/UD	-20.0	+20.0	
		Ta = 85°C ~ 105°C, V_{DD} = 3.0V	UA	-5.0	+5.0	
			UB	-8.0	+8.0	
		Ta = 105°C ~ 125°C, V_{DD} = 3.0V	UA/UB	-80.0	+10.0	
voltage coefficient	Δf/f/V	Ta = 25°C, V_{DD} = 2.2V ~ 5.5V		-1.0	+1.0	×10^{-6}/V
take-off time	TSTA	Ta = 25°C, V_{DD} = 1.5V ~ 5.5V			1.0	s
		Ta = -40°C ~ 85°C, V_{DD} = 1.5V ~ 5.5V			2.0	
age	fa	Ta = 25°C, V_{DD} = 3.0V, first year		-1.0	+1.0	×10^{-6}/year

8 electrical character

8.1 DC characteristic

Table 8-1 DC Electrical Characteristics

Unless otherwise specified, the operating conditions are: GND = 0V, V_{DD} = 1.2V to 5.5V, Ta = -40°C to 85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
current power dissipation	I_{DD1}	FOE = GND FOUT = '0'	V_{DD} = 5V		1.2	3.0	μA
	I_{DD2}		V_{DD} = 3V		0.9	2.0	
current power dissipation	I_{DD3}	FOE = V_{DD} FOUT = 32.768kHz CL = 0pF	V_{DD} = 5V		3.6		μA
	I_{DD4}		V_{DD} = 3V		2.9		
current power dissipation	I_{DD5}	FOE = V_{DD} FOUT = 32.768kHz CL = 30pF	V_{DD} = 5V		7.5		μA
	I_{DD6}		V_{DD} = 3V		6.2		
current power dissipation	I_{DD7}	During IIC communication, V_{DD} = 5V				5.0	μA
high input level	V_{IH}	FOE, SCL, SDA pins	V_{DD} = 2.2V ~ 5.5V	0.7*V_{DD}		V_{DD}+0.3	V
low input level	V_{IL}	FOE, SCL, SDA pins	V_{DD} = 2.2V ~ 5.5V	-0.3		0.3*V_{DD}	V
high output level	V_{OH}	FOUT pin	I_{OH} = -1mA	V_{DD}-0.3		V_{DD}	V
low output level	V_{OL}	FOUT, INTN pins	I_{OL} = 1mA	GND		GND+0.3	V
		SDA pin	$V_{DD} \geq 2V$ I_{OL} = 3mA	GND		GND+0.3	V
input leakage current	I_{LK}	FOE, SCL, SDA, V_{IN}=V_{DD} or GND		-0.1		0.1	μA
output leakage current	I_{OZ}	INTN, FOUT, SDA, V_{IN}=V_{DD} or GND		-0.1		0.1	μA

8.2 AC characteristic

Table 8-2 AC Electrical Characteristics

Unless otherwise specified, the operating conditions are: GND = 0V, V_{DD} = 1.5V to 5.5V, Ta = -40°C to 85°C

Item	Symbol	Condition	Standard Mode			Fast Mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	---			100			400	kHz
initial condition establishment time	$t_{SU;STA}$	---	4.7			0.6			μs
initial condition holding time	$t_{HD;STA}$	---	4.0			0.6			μs
data transfer setup time	$t_{SU;DAT}$	---	250			100			ns
data transmission hold time	$t_{HD;DAT}$	---	0			0			ns
Termination condition establishment time	$t_{SU;STO}$	---	4.0			0.6			μs
bus idle time	t_{BUF}	Between termination and initial conditions	4.7			1.3			μs
SCL low level time	t_{LOW}	---	4.0			1.0			μs
SCL high level time	t_{HIGH}	---	4.0			1.0			μs
SCL, SDA rise time	t_r	---			1.0			0.3	μs
SCL, SDA decline time	t_f	---			0.3			0.3	μs
bus spike duration	t_{SP}	---			50			50	ns
FOUT output duty cycle	Duty	Calculate the output as 50% of VDD.	40	50	60	40	50	60	%

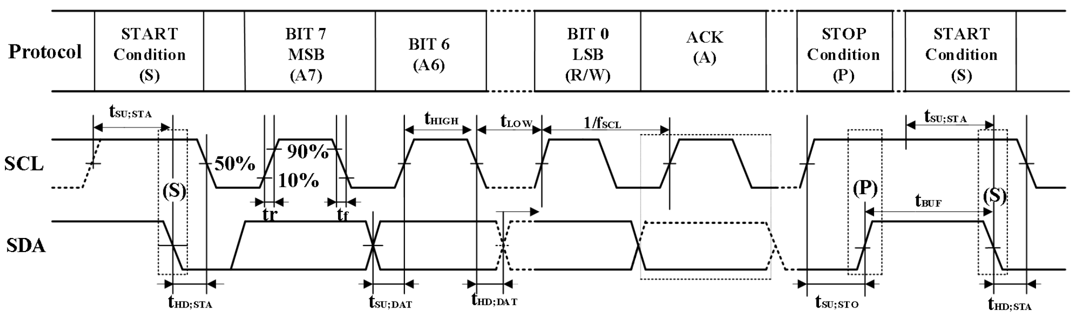


Figure 8-1 IIC timing diagram

The IIC data transfer occurs between the start and stop conditions, and must be completed within 0.95 seconds. If this time limit is exceeded, the IIC bus will be reset by the internal timer.

9 register

9.1 register table

Table 9-1 Register List

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70	MSEC[9:8]	8’h00	○	○	○	○	○	○	512	256
71	MSEC[7:0]	8’h00	128	64	32	16	8	4	2	1
00 or 10	SEC	8’h00	○	40	20	10	8	4	2	1
01 or 11	MIN	8’h00	○	40	20	10	8	4	2	1
02 or 12	HOUR	8’h00	○	○	20	10	8	4	2	1
03 or 13	WEEK	8’h40	○	6	5	4	3	2	1	0
04 or 14	DAY	8’h01	○	○	20	10	8	4	2	1
05 or 15	MONTH	8’h01	○	○	○	10	8	4	2	1
06 or 16	YEAR	8’h00	80	40	20	10	8	4	2	1
07	RAM	8’h00	●	●	●	●	●	●	●	●
08	MIN Alarm	8’h00	AE	40	20	10	8	4	2	1
09	HOUR Alarm	8’h00	AE	●	20	10	8	4	2	1
0A	WEEK Alarm	8’h00	AE	6	5	4	3	2	1	0
	DAY Alarm			●	20	10	8	4	2	1
0B or 1B	TimerCounter0	8’h00	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	8’h00	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	8’h02	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	8’h01	○	○	UF	TF	AF	○	○	XST
0F or 1F	Control	8’h42	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET
17	Temp Int	8’h00	SIGN	64	32	16	8	4	2	1
18	Temp Frac	8’h00	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
19	PW Control	8’h00	CHGEN	INIEN	○	○	○	SWSEL	SMPT1	SMPT0
1A	Offset	8’h00	○	○	○	○	OFS3	OFS2	OFS1	OFS0

Ensure valid values are written to the calendar and clock registers; otherwise, the chip cannot perform proper timing operations.

*Bits marked as ○ are read-only, with a default value of '0' and write access disabled. ●-marked bits support RAM read/write operations.

If the alarm interrupt function is not enabled (AIE = '0'), registers 8 through A can be used as RAM.

If no fixed period interrupt function is configured (TE = TIE = '0'), registers 0B or 1B,0C or 1C can be used as RAM.

The UF, TF, AF, and XST bits can only be set to '0'.

During power-up, the CSEL0 bit is set to '1', while the FSEL1, FSEL0, CSEL1, UIE, TIE, and AIE bits are set to '0'.

* MSEC[9:8] and MSEC[7:0] are read-only registers.

9.2 register specification

9.2.1 Clock and calendar registers (registers 00 – 06 or 10 – 16)

- Data format

All data except the week register (register 3) is in BCD code format. For example, the value "0101 1001" in the second register indicates the current time is 59 seconds.

The timekeeping mode is fixed to 24-hour system.

- Year Register and Leap Year

The year register's value ranges from 00 to 99, resetting to 00 after 99. A year is considered a leap year if its value is divisible by 4. The calendar's valid period spans from 2000 to 2099.

- week register

The week register has 7 valid bits (bit0 to bit6), each representing a day of the week from Monday to Sunday. Therefore, only one bit can be set to '1' in this register.

Table 9-2 Star Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

9.2.2 Millisecond registers (registers 70,71)

These two registers are read-only and cannot be written to, designed to provide millisecond-level timing for users, delivering clock accuracy beyond the second. The millisecond registers share 10 valid bits (Register 70 for the upper 2 bits, Register 71 for the lower 8 bits), with a timing precision of 1/1024 seconds.

When the user configures the second register, registers 70 and 71 are automatically reset to '0', and the timer restarts from 0ms.

9.2.3 alarm register (register 08 to 0A)

The alarm can be configured to occur at X hour and X minute on X day of each week (weekly alarm mode) or at X hour and X minute on X day of each month (daily alarm mode). The alarm mode can be set through the WADA bit in register 0D or 1D.

Each alarm register contains an AE (Alarm Enable) bit (bit7). When the AE bit of a register is '0', its set value must be compared with the corresponding timer register. If the values match, an alarm interrupt is triggered. If the AE bit is '1', the corresponding alarm register value is ignored, meaning no comparison is required with the timer register, and the register value is always considered identical to the timer register value.

When the week alarm mode is selected, multiple days of the week can be chosen simultaneously, meaning bits 0 to 6 of the WEEK ALARM function in register 0A or 1A can be set to '1' at the same time. Refer to Table 9-3 for the corresponding relationships in week alarm mode.

Table 9-3 Star Alarm Mode Register A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0A	Sunday Alarm	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

9.2.4 Fixed period counter control register (register 0B or 1B,0C or 1C)

These two registers store preset countdown values for fixed-period interrupts. When their values transition from 001h to 000h, a fixed-period interrupt occurs: TF is set to '1' and INTN outputs a low level (if TIE is '1'). Subsequently, the 0B or 1B,0C or 1C registers reset to their preset values, restarting the countdown process.

9.2.5 Control registers and flag registers (registers 0D to 0F or 1D to 1F)

- WADA position

Alarm interrupt mode selection bit: set to '1' for daily alarm mode, set to '0' for weekly alarm mode.

- USEL bit

Sets the period for time update interrupts; this bit defaults to '0' when the chip is powered on.

Table 9-4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE position

When the position is '1', the counter for fixed-period interrupts starts counting down; when it is '0', the counting stops.

- FSEL bit

This parameter sets the output frequency of the FOUT port. Refer to Table 9-5 for detailed configuration. The default value is '00' after the chip is powered on.

Table 9-5 FOUT Output Frequency Selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768kHz *Default
0	1	1024Hz
1	0	32Hz
1	1	1Hz

- TSEL bit

Sets the count period for fixed periodic interrupts.

Table 9-6 Fixed Period Interrupt Count Cycle Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF positions

These are the flag bits for alarm interrupt, fixed-period interrupt, and time update interrupt, respectively. When these interrupt events occur, the corresponding flag bits are set to '1'. The flag bits remain '1' until manually cleared to '0', and manual setting of these flag bits to '1' is prohibited.

- AIE, TIE, UIE bits

These bits are configured to control the interrupt signal output on the INTN pin during alarm interrupts, fixed-period interrupts, and time update interrupts. The default power-up state of these three bits is '0'.

The interrupt signal output on the INTN pin is a logic AND of alarm interrupt, fixed-period interrupt, and time update interrupt. The specific interrupt condition is determined by the interrupt flag, which then decides the output of the interrupt signal.

- XST bit

The stop-swing flag is set to '1' when the crystal oscillator stops oscillating, causing the clock circuit to fail in timing. This flag remains '1' until manually cleared to '0', and manual setting to '1' is prohibited. The default power-up state of this flag is '1', indicating inaccurate timing and requiring time configuration. After setting the time, the XST flag can be reset to '0' via IIC, and it will stay '0' until the crystal oscillator stops oscillating again.

- CSEL bit

Sets the time interval for the temperature compensation circuit to start. The default value is '01' (2s) after the chip is powered on.

Table 9-7 Selection of Temperature Compensation Interval

CSEL1	CSEL0	Operation interval
0	0	0.5s
0	1	2s *Default
1	0	10s
1	1	30s

- EN_DET position

The stoppage detection control bit: Setting it to '1' enables the stoppage detection function, while setting it to '0' disables it, saving approximately 50nA of circuit power. The default state of this control bit upon power-up is '1'.

- RESET bit

When RESET is set to '1', the sub-second registers are reset, the clock stops, and the temperature compensation function is disabled.

The reset bit (set to '1') will reset to '0' under three conditions: when IIC termination is detected, when a restart condition occurs, or when the IIC bus resets after 0.95 seconds.

9.2.6 Temperature register (registers 17,18)

Table 9-8 Thermometer Related Registers Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17	Temp Int	SIGN	64	32	16	8	4	2	1
18	Temp Frac	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Register 17 and 18 store the integer and decimal parts of the current temperature value respectively, where the most significant bit of register 17 is the sign bit, and the data is stored in 16-bit signed number format.

Table 9-9 Temperature Calculation Method

SIGN	Method of calculating temperature value
0	$T = reg17[6]\times 64 + \lambda + reg17[0]\times 1 + reg18[7]\times 2^{-1} + \lambda + reg18[0]\times 2^{-8}$
1	$T = reg17[6]\times 64 + \lambda + reg17[0]\times 1 + reg18[7]\times 2^{-1} + \lambda + reg18[0]\times 2^{-8} - 128$

for instance ,

The register values 0x19 and 0x80 (17,18) indicate the current temperature is 25.5°C.

The register values 17 and 18 are set to 0 FB and 0 C0 respectively, indicating the current temperature is-4.25°C.

9.2.7 Power management function register (Register 19)

Table 9-10 Power Management Function Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	PW Control	CHGEN	INIEN				SWSEL	SMPT1	SMPT0

- CHGEN position

Charging function control bit: CHGEN = '1' to enable charging; CHGEN = '0' to disable charging.

- INIEN position

Power supply automatic switching function switch. INIEN = '1' to enable automatic switching; INIEN = '0' to disable it.

- SWSEL bit

The charging switch control bit controls the on/off state between the main power supply and backup power supply in manual control mode. SWSEL = '1' turns the switch on; SWSEL = '0' turns the switch off.

- SMPT1, SMPT0 bits

Adjust the detection window size of the power control, with options of 300μs, 600μs, 2ms, or 256ms.

*For details on power management, see Chapter 10.

9.2.8 Output Precision Adjustment Register (Register 1A)

The 1A register enables fine-tuning of the output frequency for enhanced timing precision. Refer to Table 9-8 for specific adjustment ranges and step values.

Table 9-11 Output Frequency Accuracy Adjustment Table

OFS3	OFS2	OFS1	OFS0	Offset Value (ppm)
0	0	0	0	0.00
0	0	0	1	-0.55
0	0	1	0	-1.10
0	0	1	1	-1.65
0	1	0	0	-2.20
0	1	0	1	-2.75
0	1	1	0	-3.30
0	1	1	1	-3.85
1	0	0	0	4.40
1	0	0	1	3.85
1	0	1	0	3.30
1	0	1	1	2.75
1	1	0	0	2.20
1	1	0	1	1.65
1	1	1	0	1.10
1	1	1	1	0.55

10 Power management function

The JXR191T (LP)-GA features dual power supply with automatic switching capability, where the primary power source can provide trickle charging to the backup power supply.

10.1 associated register

For power management registers, refer to Section 9.2.7. Table 10-1 below details the operation modes of each control bit.

Table 10-1 Power Management Control Function Table

INIEN	CHGEN	SWSEL	SW1	Description
0	X	0	OFF (0)	Power-on initial state, single power supply
		1	ON (1)	------
1	0	X	Suitable for non-rechargeable batteries as backup power source	Automatically control the switch state based on power detection results, following the power management control flow.
	1		Applicable as backup power source for rechargeable batteries	

10.2 power supply detection module

To meet the requirements of dual power supply control, the chip has two independent power detection units, which are used to detect whether the rechargeable battery is fully charged and whether the main power supply voltage is higher than the backup power supply.

Table 10-2 Power Management Control Function Table

Symbol Name	Description
VD2	Check the voltage of V_{BAT} and V_{FULL} (3.7V). If V_{BAT} is higher, the output is '1'.
VD3	Check the voltage levels of V_{BAT} and V_{DD}. If V_{BAT} is higher, the output is '1'.

10.3 Default state of power supply

The default power management configuration is illustrated in Figure 10-1. The V_{BAT} is directly connected to the RTC power supply, while V_{DD} is linked to the RTC power supply via a diode. For single-power operation, it is recommended to either power the V_{BAT} directly or short-circuit the V_{BAT} to V_{DD}.

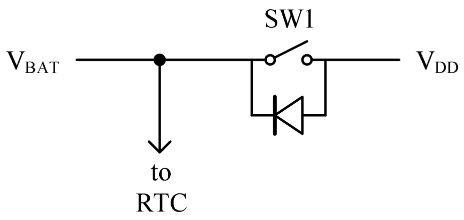


Figure 10-1 Default power state upon power-on

10.4 single power supply

As specified in Section 10.3, when the chip is powered by a single power supply, it is recommended to use V_{BAT} for power supply or short-circuit V_{BAT} to V_{DD}.

10.5 Non-rechargeable batteries as backup power sources

When the backup power source is a non-rechargeable battery, set INIEN to '1' to enable automatic power switching, and set CHGEN to '0' to disable charging. Refer to Table 10-3 for the specific control method.

Table 10-3 Control Table for Non-Rechargeable Batteries as Standby Power Sources

Power supply test results	SW1	Power supply status
$V_{DD} > V_{BAT}$	ON	main power supply
$V_{DD} < V_{BAT}$	OFF	Backup power supply

10.6 Rechargeable batteries as backup power sources

When using rechargeable batteries as backup power, set INIEN to '1' to enable automatic power switching and CHGEN to '1' to activate charging. The system automatically switches power supply based on two power detection pairs (V_{BAT} vs V_{DD}, V_{BAT} vs V_{FULL}), where V_{FULL} is the cutoff voltage for backup power (approximately 3.7V). The switch control states are detailed in Table 10-4.

Table 10-4 Control Table for Rechargeable Batteries as Standby Power Sources

Power supply test results		SW1	charged state	Power supply status
$V_{DD} < V_{BAT}$		OFF	stop charge	Backup power supply
$V_{DD} > V_{BAT}$	$V_{BAT} \geq V_{FULL}$	OFF	stop charge	main power supply
	$V_{BAT} < V_{FULL}$	ON	charge	main power supply

To ensure the accuracy of the power detection results, the circuit must disconnect the switch SW1 during testing. The detection window size is determined by the SMPT1 and SMPT0 registers.

Table 10-5 Power Supply Detection Window Control Table

SMPT1	SMPT0	detection window
0	0	300us *Default
0	1	600us
1	0	2ms
1	1	256ms

10.7 power management control flow

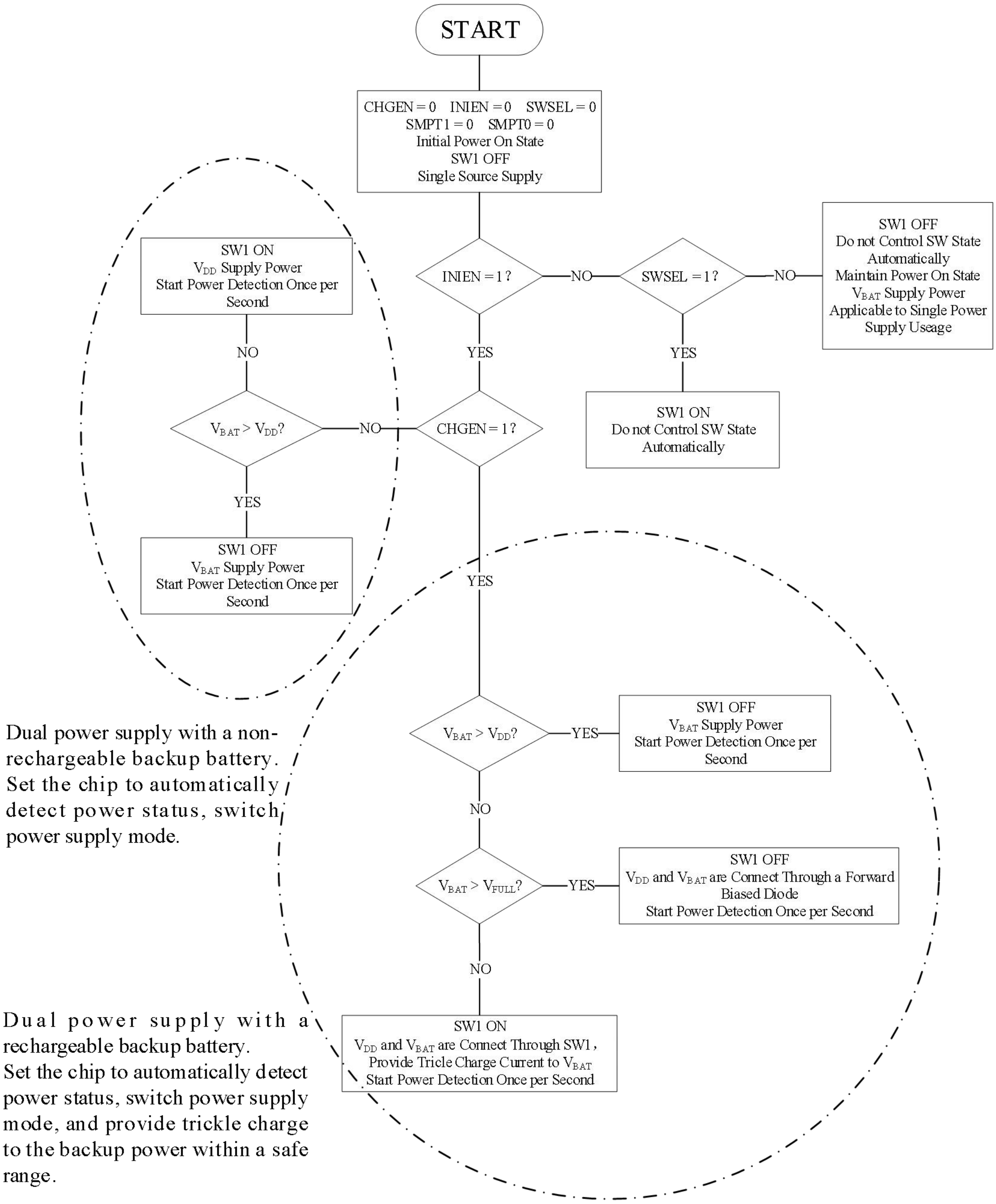


Figure 10-2 Workflow diagram of the power management module

11 interrupt capability

11.1 alarm interrupt

Alarm interrupts can occur on specified days, hours, or minutes.

11.1.1 alarm interrupt timing

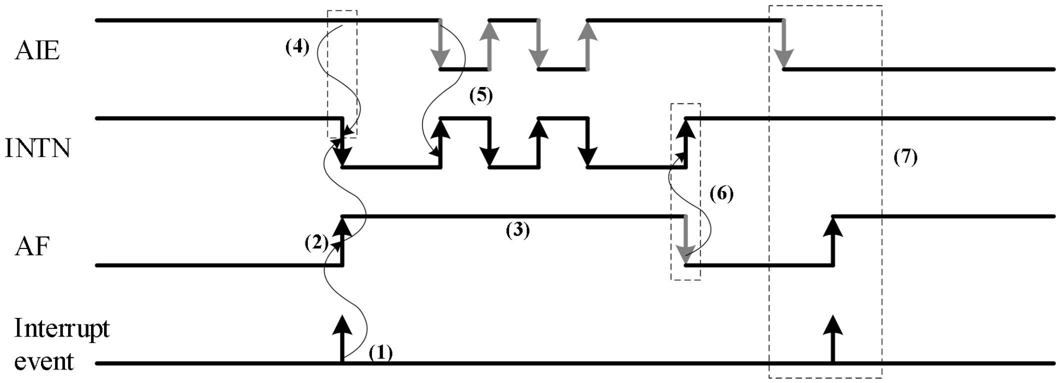


Figure 11-1 Alarm Interrupt Sequence

(1) Set the alarm interrupt to match the hour, minute, date, or day of the week, along with the WADA register. When the set time matches the current time, an alarm interrupt event is triggered.

(2) When an alarm interrupt occurs, the AF flag is set to '1'.

(3) The AF register remains at '1' until manually cleared to '0'.

(4) When an alarm interrupt occurs, INTN outputs low if AIE is '1', and remains high if AIE is '0'.

(5) When INTN = '0', setting AIE to '0' immediately restores INTN to high-impedance state. AIE can control INTN's output state until an alarm interrupt occurs and the AF register is cleared to' 0'.

(6) Clearing the AF register to '0' deactivates the alarm interrupt output, causing INTN to immediately transition from '0' to a high-impedance state.

(7) When an alarm interrupt occurs, if AIE equals '0', INTN remains in a high-impedance state and does not output a low level.

11.1.2 alarm interrupt related register

Table 11-1 Alarm Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D or 1D	Extension	○	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	**AF**	○	○	XTS
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	**AIE**	○	EN_DET	RESET

- When configuring the alarm interrupt register, it is recommended to set AIE to '0' first to prevent unnecessary hardware interrupts during the operation.
- WADA selects alarm mode: '1' for daily alarm, '0' for weekly alarm.
- An alarm interrupt event sets the AF flag to '1', which remains set until manually reset to '0'.
- When an alarm interrupt occurs, the AIE determines whether to generate an interrupt signal output (if AIE = '1', INTN = '0'; if AIE = '0', INTN = Hi-Z).
- A '0' in the AE bit indicates that the corresponding register must be compared with the clock or calendar register. If the AE bit is '1', the register is not compared, meaning it is always kept synchronized with the clock or calendar register. See the example below:
  (1) When register 0A is set to '80', only the minute and hour alarm registers need to be compared with their corresponding clock registers, while the day/month/week register is ignored. Thus, as long as the hour and minute registers match, an alarm interrupt event will occur every day.
  (2) Setting the AEs in registers 08,09, and 0A to '1' will trigger an alarm interrupt every minute.

11.2 fixed periodic interrupt

The fixed period interrupt can produce alarm events between 244.14μs and 4095min according to a fixed period.

11.2.1 fixed period interrupt timing

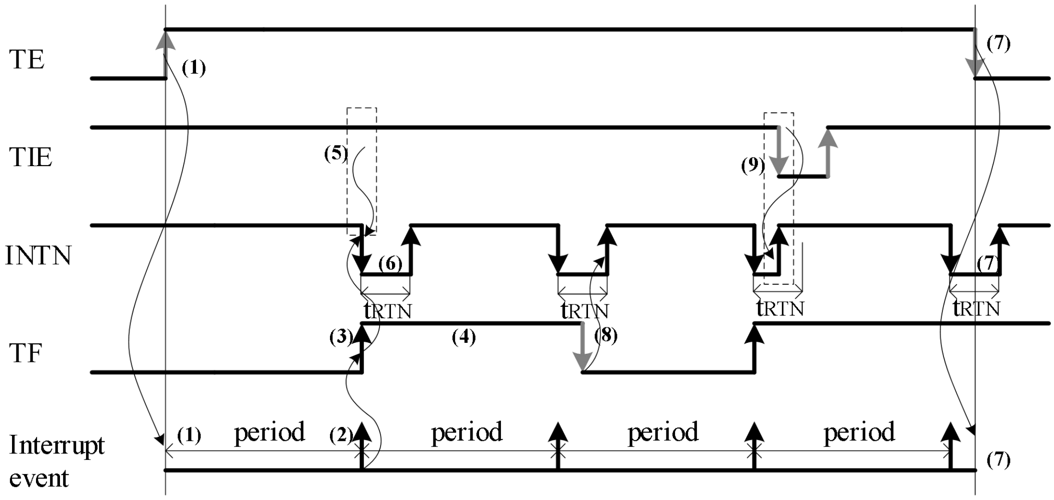


Figure 11-2 Fixed Period Interrupt Timing

(1) When the TE bit is set to '1', the fixed-period counter starts counting down from its preset value.

(2) An interrupt event is generated when the fixed-period counter counts from 001h to 000h. The counter resets to its preset value and continues counting.

(3) When a fixed-period interrupt occurs, the TF register is set to '1'.

(4) The TF register remains at '1' until manually cleared to '0'.

(5) When a fixed-period interrupt event occurs, INTN outputs a low level if TIE is '1', and remains high-impedance if TIE is '0'.

(6) The INTN output remains low for tRTN duration, then automatically reverts to high-impedance state until the next interrupt signal is triggered.

(7) When the TE bit is set to '0', the fixed-period counter stops counting, and INTN outputs high impedance. If the TE bit is set to '0' during INTN = '0', INTN will return to high impedance after the tRTN time.

(8) If TF is cleared to '0' during INTN = '0', it will revert to high-resistance state after INTN persists for tRTN duration.

(9) When TIE is set to '0', INTN immediately returns to high-impedance state. If TIE is reset to '1' during the tRTN period, INTN remains low-level until the tRTN ends.

11.2.2 fixed period interrupt related register

Table 11-2 Fixed Period Interrupt-Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	TimerCounter0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C or 1C	TimerCounter1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D or 1D	Extension	○	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0E or 1E	Flag	○	○	UF	**TF**	AF	○		XST
0F or 1F	Control	CSEL1	CSEL0	UIE	**TIE**	AIE	○	EN_DET	RESET

- When configuring fixed-period interrupt registers, it is recommended to first set both TE and TIE to '0' to prevent unnecessary hardware interrupts during operation.
- TSEL1 and TSEL0 are used to set the fixed-period interrupt countdown cycles, with the interrupt signal on the INTN pin's auto-reset time being synchronized to these cycles.

Table 11-3 Fixed Period Interrupt Counting Period and Automatic Reset Time

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122ms
0	1	64Hz	7.8125ms
1	0	1Hz	7.8125ms
1	1	1/60Hz	7.8125ms

- Register 0B or 1B,0C or 1C sets the default value of the counter (001h to FFFh). The counter counts down to 000h at the TSEL-defined cycle, triggering a fixed-period interrupt event.
- TE is the enable control bit of the fixed-period counter. When TE is set to '1', the counter starts counting down; when TE is '0', the counter stops counting, terminating the fixed-period interrupt function.
- The occurrence of periodic cycle interrupt events sets the TF flag to '1', which remains set until manually cleared to '0'.
- When a fixed-period interrupt event occurs, TIE determines whether to generate an interrupt signal output (if TIE = '1', INTN = '0'; if TIE = '0', INTN = Hi-Z).

Table 11-4 Example of Fixed Period Interrupt Period

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
……	……	……	……	……
2048	500ms	32s	2048s	2048min
……	……	……	……	……
4095	0.9998s	63.984s	4095s	4095min

11.3 Time update interrupted

Based on the set value, the time update interrupt generates alarm events at second or minute intervals.

11.3.1 interrupt timing of time update

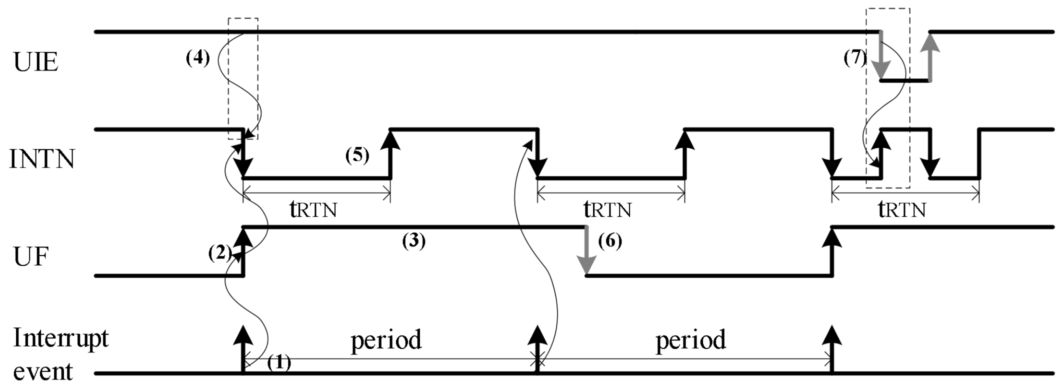


Figure 11-3 Time Update Interrupt Sequence

(1) The USEL register determines whether the chip is in second or minute update interrupt mode. When the corresponding second or minute register updates, a time update interrupt event is generated.

(2) When the time update interrupt occurs, the UF register is set to '1'.

(3) The UF register will remain at '1' until manually cleared to '0'.

(4) When a time update interrupt event occurs, if UIE = '1', INTN outputs a low level; if UIE = '0', INTN remains in a high-impedance state.

(5) The INTN output remains low for tRTN duration, then automatically reverts to high-impedance state until the next interrupt signal is triggered.

(6) If the UF is cleared to '0' during the INTN = '0' period, INTN will revert to the high-resistance state after the tRTN time.

(7) If the UIE is set to '0' during the INTN = '0' period, INTN immediately returns to the high-impedance state, terminating the interrupt signal output. If the UIE is reset to '1' again during the tRTN period, INTN reverts to the low-level state until the end of tRTN.

11.3.2 time update interrupt register

Table 11-5 Time Update Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	○	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	**UF**	TF	AF	○	○	VDET
0F or 1F	Control	CSEL1	CSEL0	**UIE**	TIE	AIE	○	EN_DET	RESET

- When configuring the timer interrupt register, set the UIE to '0' first to prevent unnecessary hardware interrupts during operation.
- The USEL signal is used to set the interrupt mode to second or minute updates.

Table 11-6 Time Update Interrupt Mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event sets the UF flag to '1', which remains set until manually cleared to '0'.
- When a time update interrupt event occurs, the UIE determines whether to generate an interrupt signal output (if UIE = '1', INTN = '0'; if UIE = '0', INTN = Hi-Z).

12 IIC BI

12.1 Characteristics of IIC Bus

The IIC is a bidirectional communication interface where the signal line (SDA) and clock line (SCL) are connected to VDD via pull-up resistors. The IIC bus port must be configured as an open-drain structure to enable multi-device wiring and connection.

12.2 data transmission

Each SCL clock cycle transmits 1bit of data. During transmission, data on the SDA line changes when the SCL is at low level; during reception, stable and valid data can be obtained from the SDA line when the SCL is at high level.

12.3 Start and Stop conditions

In idle state, both SCL and SDA remain at high level. When SCL is high, the falling edge of SDA initiates IIC communication, while its rising edge terminates it.

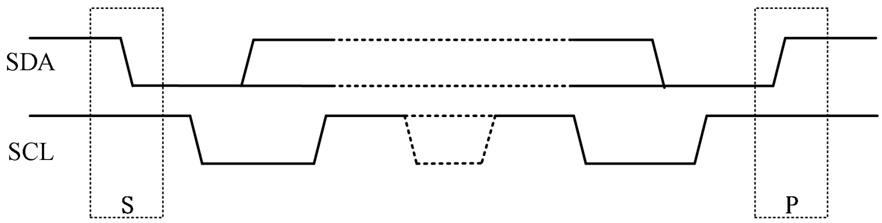


Figure 12-1 Start and Stop conditions of IIC

12.4 Select device (slave address)

The IIC bus lacks a chip select signal. The master device selects a slave device by sending a unique fixed device number (slave address), and the selected slave device responds to establish communication with the master.

The address consists of 7 bits of data, with 4 bits (Group 1) and 3 bits (Group 2). The slave address for JXR191T (LP)-GA is "0110010". During communication, the slave address and read/write selection bit are transmitted as 8-bit data.

Slave address							R/W bit
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	1	0	R/W

0:write mode
1:read mode

Figure 12-2 IIC Address Schematic

12.5 system configuration

The device that controls the data transmission is called the master device, the device controlled by the master device is called the slave device, the device that sends the data is called the sender, the device that receives the data is called the receiver.

In the JXR191T (LP)-GA system, the CPU or other control devices act as master devices, while the JXR191T (LP)-GA chip itself serves as a slave device. Both master and slave devices can function as either the transmitter or receiver.

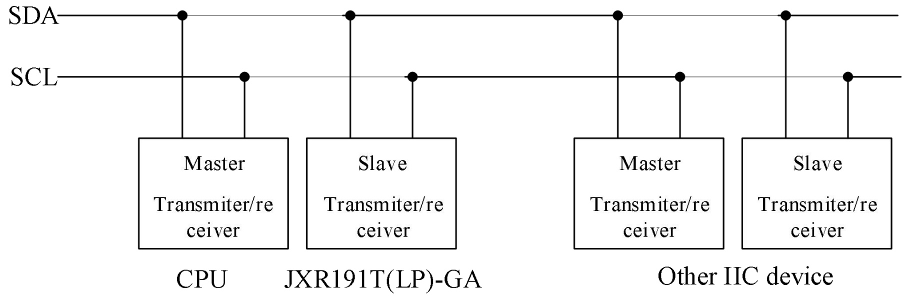


Figure 12-3 IIC System Configuration

12.6 acknowledge signal

The IIC bus imposes no restrictions on the number of bytes transmitted between start and stop conditions. Upon completion of each byte transfer, the transmitter must release the SDA bus and provide one SCL clock to receive the acknowledge signal. If the receiver successfully receives 8-bit data, it must set the SDA to '0' after the clock cycle of the final 1-bit data transmission. The transmitter then interprets this low level as the successful acknowledge signal. One clock cycle later, the receiver releases the SDA bus and prepares to receive new data.

The IIC bus terminates data transmission when the following conditions are met:

(1) When the master device acts as the transmitter, it terminates the transmission upon receiving the acknowledge signal from the slave device.

(2) When the main device acts as the receiver, it sends a '1' as the acknowledge signal after successfully receiving 8-bit data, followed by the termination condition.

12.7 IIC bus control

This section describes the IIC bus communication timing when the CPU acts as the master device and the JXR191T (LP)-GA as the slave device.

12.7.1 addressed write operation

The JXR191T (LP) -GA features an auto-increment address system. Once the target address is set, it only requires continuous data transmission, with the address bit incrementing automatically.

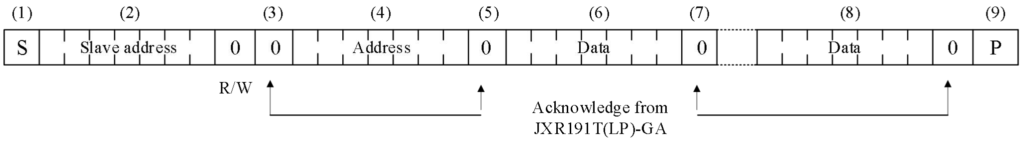


Figure 12-4 specifies the address write operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR191T (LP)-GA slave address and sets the R/W bit to write mode.

(3) JXR191T (LP)-GA sends the acknowledge signal.

(4) The CPU sends the write register address to JXR191T (LP)-GA.

(5) JXR191T (LP)-GA sends the acknowledge signal.

(6) The CPU sends data to the register at the specified address in (4).

(7) JXR191T (LP)-GA sends the acknowledge signal.

(8) Repeat steps (6) and (7), where the address of the write register in JXR191T (LP)-GA will increment automatically.

(9) The CPU sends the stop bit [P].

12.7.2 addressed read operation

After writing to the register, the CPU can read the register data by setting the read mode.

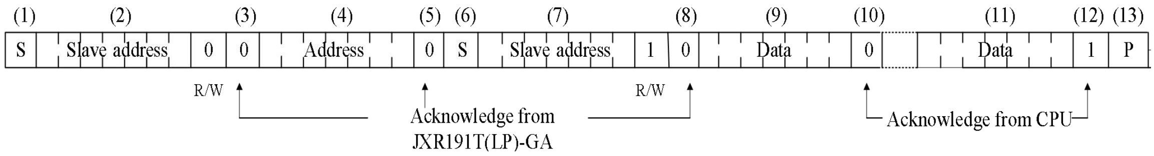


Figure 12-5 Specified Address Read Operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR191T (LP)-GA slave address and sets the R/W bit to write mode.

(3) JXR191T (LP)-GA sends the acknowledge signal.

(4) The CPU sends the read register address to JXR191T (LP)-GA.

(5) JXR191T (LP)-GA sends the acknowledge signal.

(6) The CPU sends the restart bit.

(7) The CPU sends the JXR191T (LP)-GA slave address and sets the read mode via the read/write (R/W) bit.

(8) JXR191T (LP)-GA sends the acknowledge signal, then the CPU acting as the receiver and JXR191T (LP)-GA as the transmitter.

(9) The JXR191T (LP) -GA sends the data from the register at the specified address in (4).

(10) The CPU sends the acknowledge signal to JXR191T (LP)-GA.

(11) Repeat steps (9) and (10), where the address of the read register in JXR191T (LP)-GA will increment automatically.

(12) The CPU sends the acknowledge signal to JXR191T (LP)-GA.

(13) The CPU sends the stop bit [P].

12.7.3 Unspecified address read operation

The master device can directly enter read mode to access the register contents of the slave device. As the master device does not specify the read operation address, the slave device starts reading from the address one unit higher than the previous IIC operation address.

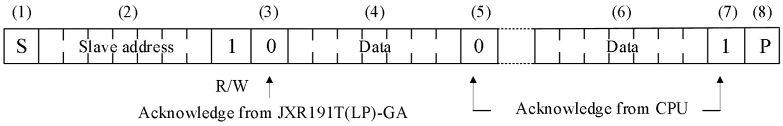


Figure 12-6 Unspecified address read operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR191T (LP)-GA slave address and sets the read mode via the read/write (R/W) bit.

(3) JXR191T (LP)-GA sends the acknowledge signal, then the CPU acting as the receiver and JXR191T (LP)-GA as the transmitter.

(4) The JXR191T (LP) -GA automatically increments the register address and sends the register data.

(5) The CPU sends the acknowledge signal to JXR191T (LP)-GA.

(6) When repeating steps (4) and (5), the address of the read register in JXR191T (LP)-GA will increment automatically.

(7) The CPU sends the acknowledge signal to JXR191T (LP)-GA.

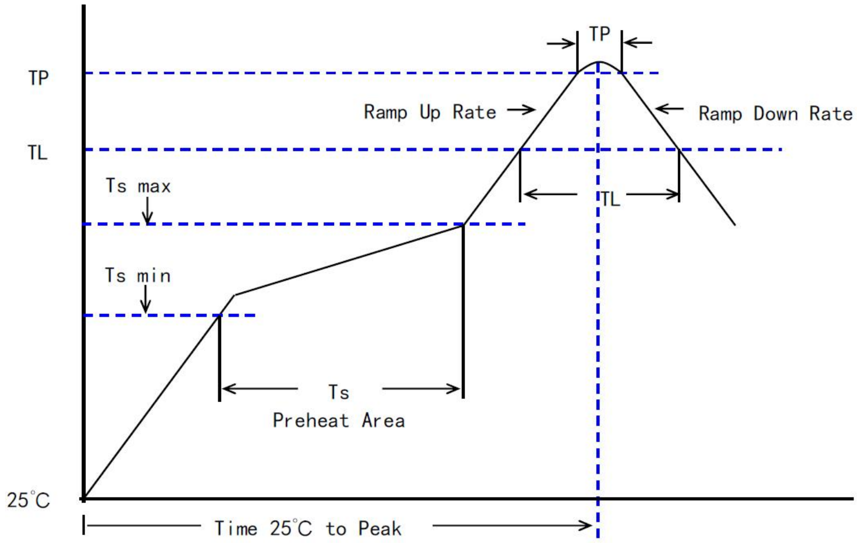
(8) The CPU sends the stop bit [P].

Appendix

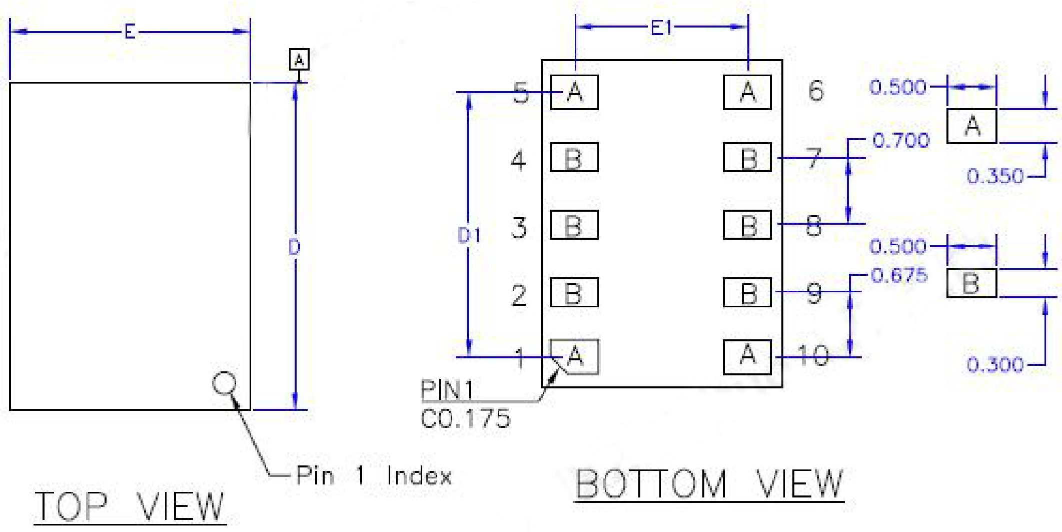
direction for use

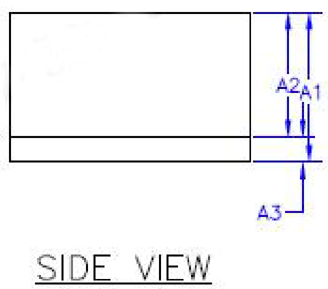
1. The product features an electrostatic protection rating of HBM ±2.0kV and CDM ±2.0kV. During operation, precautions must be taken to prevent electrostatic discharge.
2. During operation, power spikes exceeding 8.25V may trigger latch-up effects and circuit damage. To ensure stable chip operation, install a decoupling capacitor (minimum 0.1uF) near the clock chip's power pin.
3. Because the clock chip is a low power integrated circuit, it is necessary to avoid placing any high noise components around the clock chip.
4. Floating input pins on a chip may increase current power consumption. During operation, the input pins should be connected to a fixed potential (V_{DD} or GND).
5. The chip's humidity sensitivity rating is Level 3. From unpacking to board soldering, the workshop storage environment must maintain temperature and humidity below 30°C and 60%RH respectively, with a maximum storage duration of 168 hours.
6. During reflow soldering, the peak temperature must be strictly controlled to not exceed 260°C, with a maximum of two reflow cycles allowed. Manual soldering should not exceed 350°C, and the soldering duration should not exceed 5 seconds. Failure to comply may damage the built-in crystal oscillator, causing excessive clock deviation or even complete stoppage. Refer to the reflow curve diagram below for guidance.

Profiles Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts Min) Temperature Max (Ts Max) Time (Ts) from (Ts Min to Ts Max)	 150℃ 200℃ 60 ~ 120 seconds
Ramp-up rate (TL to TP)	3℃/second Max
Liquidous Temperature (TL) Time (TL) maintained above TL	217℃ 35 seconds Max
Peak/Classification Temperature (TP)	245±5℃
Time within 5℃ of actual Peak Temperature (TP)	5 seconds Max
Ramp-down rate (TP to TL)	6℃/second Max
Time 25℃ to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max



Package size

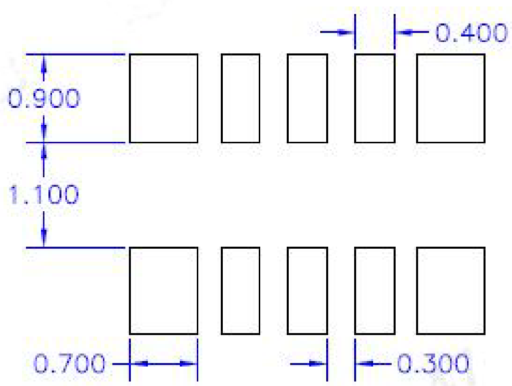




Dimensional Ref.

REF.	Min.	Nom.	Max.
A1	1.50	1.56	1.62
A2	1.30 BSC		
A3	0.22	0.26	0.30
D	3.30	3.40	3.50
E	2.40	2.50	2.60
D1	2.75 BSC		
E1	1.80 BSC		

Recommended soldering pattern



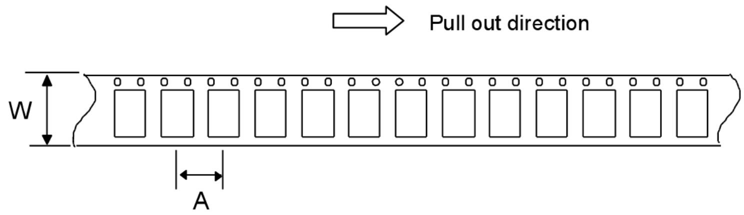
Unit : mm

Packing specifications

Emboss Taping (TE2)

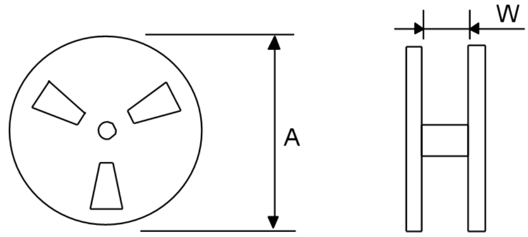
Symbol	LGA10
A	4
W	12

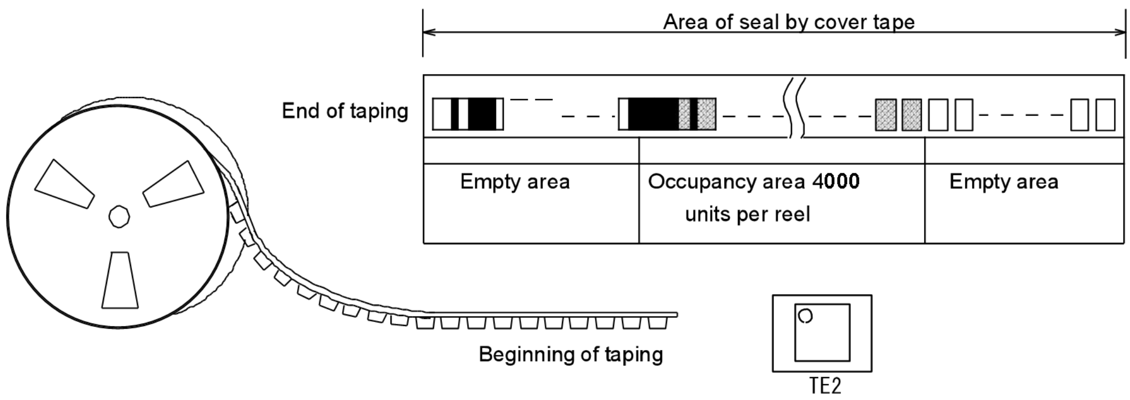
Unit : mm

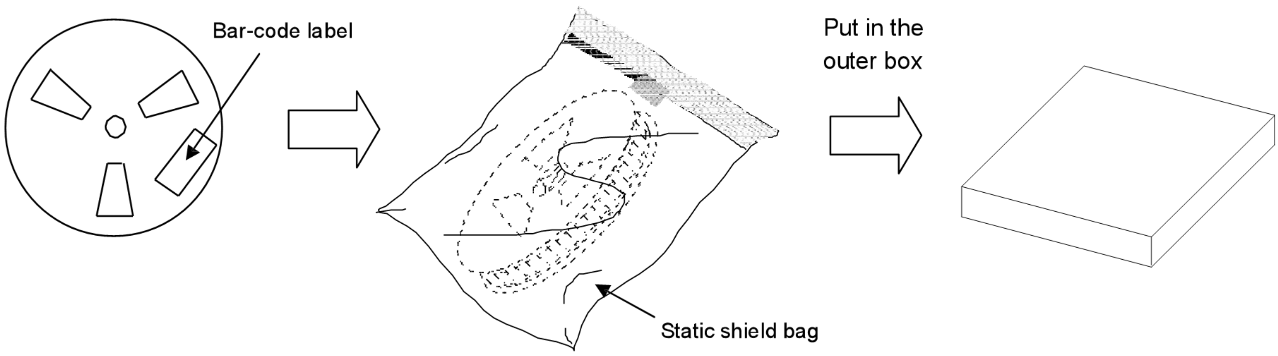


Symbol	LGA10
A	330
W	12.4

Unit : mm

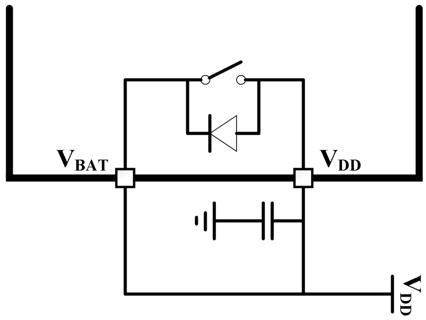




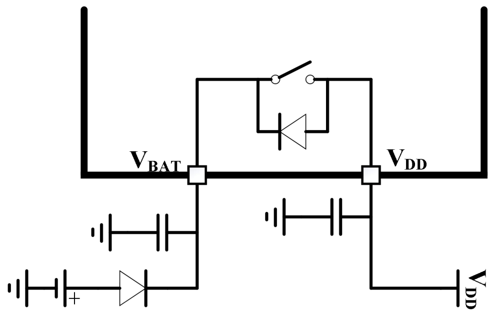


Power connection example

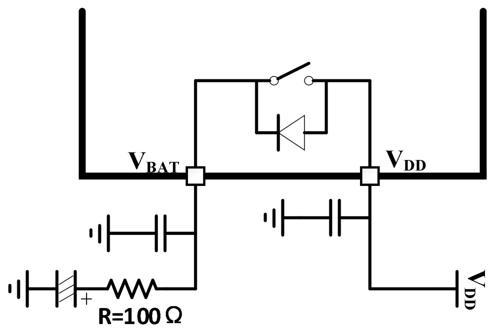
In systems without backup power, connect both V_{DD} and V_{BAT} to the external power supply, and the PW Control register will retain its default configuration.



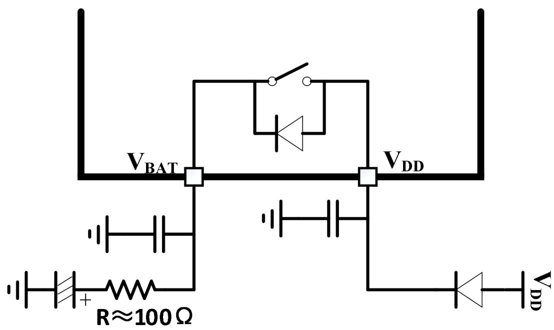
When the backup power supply uses non-rechargeable batteries, an external Schottky diode must be connected to prevent battery charging. In the event of V_{DD} power failure, a maximum of 1 second may exist as a leakage path from V_{BAT} to V_{DD}.



When using rechargeable batteries as backup power, a 100-ohm resistor should be connected in series with the battery to prevent voltage spikes during power switching. Additionally, in the event of V_{DD} power loss, a leakage path from V_{BAT} to V_{DD} may persist for up to 1 second.



To limit the charging current of rechargeable batteries, a 100-ohm current-limiting resistor can be connected in series. To prevent leakage paths from V_{BAT} to V_{DD}, a Schottky diode can be connected in series at the V_{DD} terminal.



Order Information

product name	material number	Package form	Packaging format	Minimum order quantity
JXR191T(LP)-GA (UA)	OSC05191TLPA1000	LGA10	13-inch reel	4000
JXR191T(LP)-GA (UB)	OSC05191TLPA2000	LGA10	13-inch reel	4000
JXR191T(LP)-GA (UC)	OSC05191TLPA3000	LGA10	13-inch reel	4000
JXR191T(LP)-GA (UD)	OSC05191TLPA4000	LGA10	13-inch reel	4000

Product Label Description