JXR2060 User Manual

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catalogue

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1 summary

The JXR2060 is a low-power real-time clock chip featuring a built-in frequency offset correction register, enabling software-based frequency adjustment. It supports the standard IIC communication protocol up to 400kHz and offers flexible interrupt output configurations with adjustable clock frequencies.

2 characteristic

- The real-time clock function provides information including year/month/day/week/hour/minute /second based on a 32.768kHz crystal oscillator.
- The clock circuit operates within a voltage range of 0.9V to 5.5V.
- Low current power consumption: 0.6μA@3.3V/25℃
- Supports the 400kHz standard IIC interface protocol (operating voltage range: 1.5V to 5.5V)
- Programmable output clock frequencies: 32.768kHz, 16.384kHz, 8.192kHz, 4.096kHz, 2.048kHz, 1.024kHz, and 1Hz
- Built-in crystal oscillator with load capacitor, supporting optional 7pF/12.5pF configurations
- Alarm interrupt (alarm clock) function
- Fixed cycle interrupt function
- 1.5-minute timer interrupt function
- Built-in clock stop detection circuit
- built-in power-on reset circuit
- The timing accuracy can be calibrated by adjusting the Offset register through software.

3 application area

- digital camera
- printer
- mobile devices
- automotive electronics
- Network devices such as routers
- Various battery-powered devices

4 structured flowchart

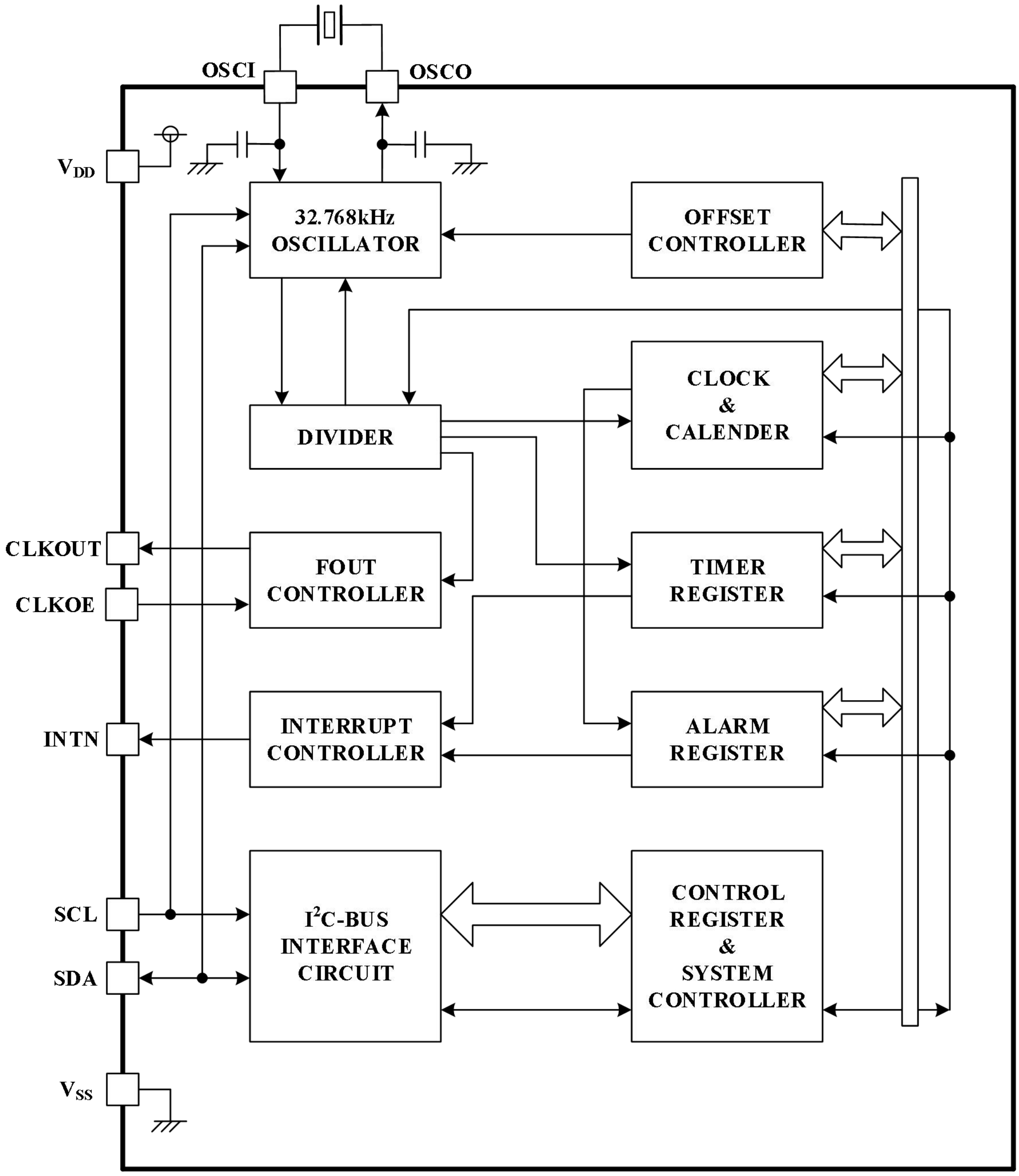


Figure 4-1 Block diagram of the JXR2060 system

5 Pin definition

5.1 package form

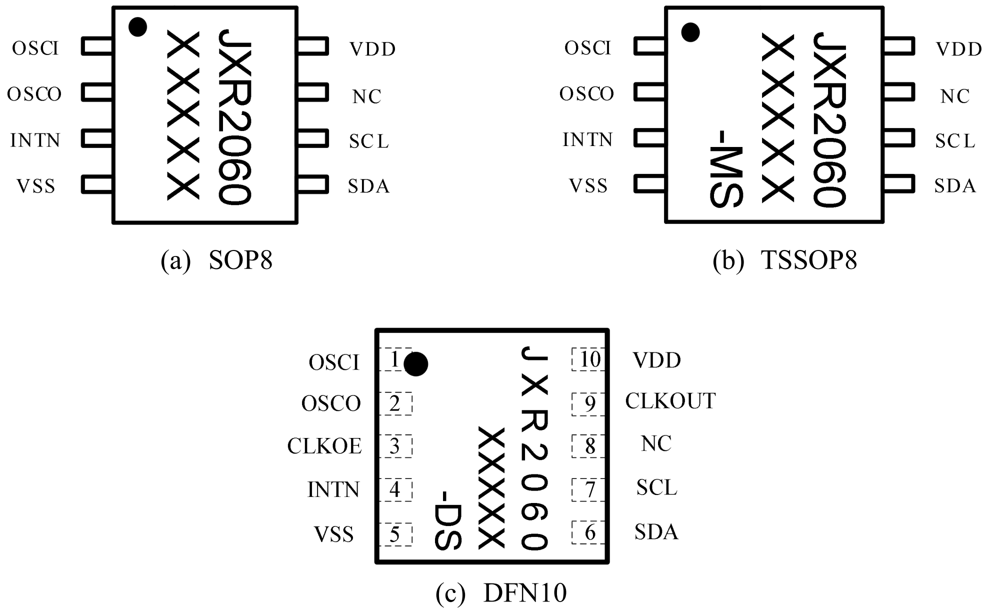


Figure 5-1 JXR2060 package form

5.2 Pin functions

Table 5-1 JXR2060 Pin Definition

Pin name	Pin No.			Type	Description
	JXR2060	JXR2060-DS	JXR2060-MS		
OSCI	1	1	1	input	crystal oscillator input
OSCO	2	2	2	output	output of crystal oscillator
CLKOE	-	3	-	input	The frequency control pin outputs the CLKOUT frequency when set to 1.
INTN	3	4	3	output	Interrupt output pin, N-Ch open drain structure
V_{SS}	4	5	4	ground	earth wire
SDA	5	6	5	inout	IIC bus communication data transmission end, N-channel open drain output
SCL	6	7	6	input	IIC bus communication clock transmission terminal
N.C.	-	8	-	-	Keep suspended
CLKOUT	-	9	-	output	Clock output pin, push-pull output
V_{DD}	8	10	8	power	Power supply terminal

6 absolute maximum rating

Table 6-1 Absolute Maximum Rated Value

Item	Symbol	Condition	Rating	Unit
Power Supply Voltage*1	V_{DD}	Voltage between V_{DD} and V_{SS}	-0.5 to 6	V
Input voltage *1, *2	V_{IN}	SCL, SDA, CLKOE pins	-0.5 to V_{DD}+0.5	V
Output voltage*1, *2	V_{OUT}	CLKOUT, SDA, INTN pins	-0.5 to V_{DD}+0.5	V
storage temperature	T_{STG}	Dispersed storage, unpackaged	-65 to 150	℃

*1: All electrical parameters must never exceed the maximum rated values specified in the table. Exceeding these limits may degrade performance, reduce reliability, or even cause chip failure.

*2: Here, V_{DD} denotes the recommended operating voltage range.

7 Recommended operating conditions

Table 7-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
control voltage	V_{DD}	port operation voltage	1.5	3.0	5.5	V
clock operating voltage	V_{CLK}	clock circuit operating voltage	0.9	3.0	5.5	V
maximum pull-up voltage	V_{PUP}	SDA, INTN pins			5.5	V
service temperature	T_{OPR}	---	-40	25	85	℃

Any operation beyond the recommended range in the table may significantly compromise the chip's reliability.

8 frequency characteristic

Table 8-1 Frequency Characteristics

Item	symbol	Condition	Min.	Typ.	Max.	Unit
output frequency	fo			32.768(Typ)		kHz
voltage coefficient	Δf/f/V	Ta = 25°C, V_{DD} = 1.1V~5.5V	-1.0		+1.0	$\times 10^{-6}$/V
built-in load capacitance	C_L	7pF crystal oscillator	4.2	7	9.8	$\times 10^{-6}$
		12.5pF crystal oscillator	7.5	12.5	17.5	
Start-up time	T_{STA}	Ta = 0 °C ~ 50 °C VDD = 1.5V ~ 5.5V			1.0	s
		Ta = -40 °C ~ 85°C VDD = 1.5V ~ 5.5V			3.0	
ESR driving capability	RESR	---			150	kΩ

9 electrical character

9.1 DC characteristic

Table 9-1 DC Electrical Characteristics

Unless otherwise specified, the operating conditions are: VSS = 0V, VDD = 1.5V to 5.5V, and Ta = -40°C to 85°C.

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
current power dissipation	I_{DD1}	IIC Frequency 400kHz			1.5	3.0	μA
	I_{DD2}	IICFrequency100kHz			1.2	2.5	
	I_{DD3}	Without IIC Communication and CLKOUT Frequency Output @25°C	V_{DD}=5V		700	1400	nA
	I_{DD4}		V_{DD}=3V		600	1200	
	I_{DD5}	Without IIC Communication and CLKOUT Frequency output @-40°C~85°C	V_{DD}=5V		750	1500	
	I_{DD6}		V_{DD}=3V		650	1300	
high input level	V_{IH}	SCL, SDA , CLKOE pins		0.7*V_{DD}		V_{DD}	V
low input level	V_{IL}			-0.5		0.3*V_{DD}	V
low output level	V_{OL}	CLKOUT, INTN, SDA pins	I_{OL}=1mA	0		0.4	V
low output current	I_{OL}	Pull down current@V_{DD}=5V, V_{OL}=0.4V	SDA pin	3			mA
			INTN pin	1			
			CLKOUT pin	1			
input leakage current	I_{LK}	SCL, SDA, CLKOE pins, V_{IN}=V_{DD} or V_{SS}		-0.3		0.3	μA
output leakage current	I_{OZ}	INTN, CLKOU, SDA pins, V_{IN}=V_{DD} or V_{SS}		-0.3		0.3	μA

9.2 AC characteristic

Table 9-2 AC Electrical Characteristics

*Unless otherwise specified, the operating conditions are: V_{SS} = 0V, V_{DD} = 1.5V to 5.5V, Ta = -40°C to 85°C, f_{SCL} = 400kHz

Item	Symbol	Condition	Standard Mode			Fast Mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	---			100			400	kHz
initial condition establishment time	$t_{SU;STA}$	---	4.7			0.6			μs
initial condition holding time	$t_{HD;STA}$	---	4.0			0.6			μs
data transfer setup time	$t_{SU;DAT}$	---	250			100			ns
data transmission hold time	$t_{HD;DAT}$	---	0			0			ns
Termination condition establishment time	$t_{SU;STO}$	---	4.0			0.6			μs
bus idle time	t_{BUF}	Between Start bit and Stop bit	4.7			1.3			μs
SCL low level time	t_{LOW}	---	4.0			1.0			μs
SCL high level time	t_{HIGH}	---	4.0			1.0			μs
SCL, SDA rise time	t_r	---			1.0			0.3	μs
SCL, SDA decline time	t_f	---			0.3			0.3	μs
bus spike duration	t_{SP}	---			50			50	ns
FOUT output duty cycle	Duty	Calculate the output as 50% of V_{DD}.	40	50	60	40	50	60	%

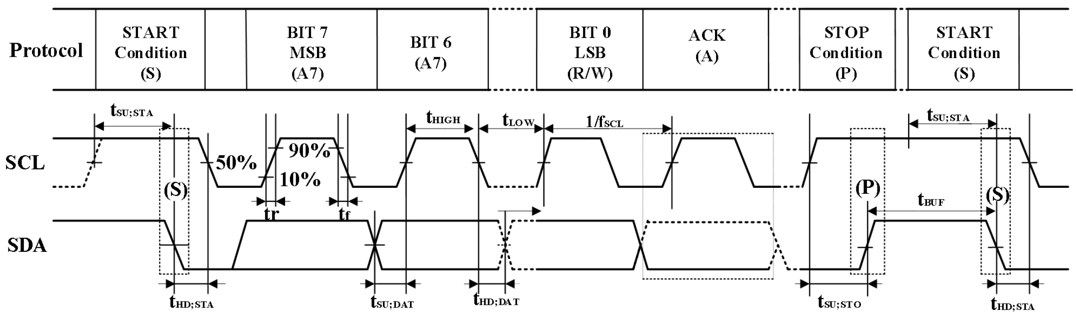


Figure 9-1 IIC timing diagram

The IIC data transfer occurs between the start and stop conditions, and must be completed within 0.95 seconds. If this time limit is exceeded, the built-in timer will reset the IIC bus.

10 register

10.1 register table

Table 10-1 Register List

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control and Status registers										
00	Ctrl0	8' h00	EXT_TEST	○	STOP	SR	○	CIE	12_24	CAP_SEL
01	Ctrl1	8' h00	AIE	AF	MI	HMI	TF	COF[2:0]		
02	Offset	8' h00	MODE	OFFSET[6:0]						
03	RAM	8' h00	B[7:0]							
RTC registers										
04	SEC	8' h80	OS	40	20	10	8	4	2	1
05	MIN	8' h00	○	40	20	10	8	4	2	1
06	HOUR	8' h00	○	○	20	10	8	4	2	1
			○	○	AM/PM	10	8	4	2	1
07	DAY	8' h01	○	○	20	10	8	4	2	1
08	WEEK	8' h06	○	○	○	○	○	4	2	1
09	MONTH	8' h01	○	○	○	10	8	4	2	1
0A	YEAR	8' h00	80	40	20	10	8	4	2	1
Alarm registers										
0B	SEC Alarm	8' h80	AEN_S	40	20	10	8	4	2	1
0C	MIN Alarm	8' h80	AEN_M	40	20	10	8	4	2	1
0D	HOUR Alarm	8' h80	AEN_H	○	20	10	8	4	2	1
				○	AM/PM	10	8	4	2	1
0E	DAY Alarm	8' h80	AEN_D	○	20	10	8	4	2	1
0F	WEEK Alarm	8' h80	AEN_W	○	○	○	○	4	2	1
Timer registers										
10	Timer Value	8' h00	128	64	32	16	8	4	2	1
11	Timer Mode	8' h18	○	○	○	TCF[1:0]		TE	TIE	TI_TP

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12	Setting	8' h06	○	●	●	●	●	DET_EN	ADJ[1:0]	

Ensure that valid values are written to the calendar and clock registers; otherwise, the chip cannot perform proper timing operations.

*The register bits marked with ○ are read-only, and the value is 1'b0.

* Register bits marked with ● can be used as RAM.

After completing the read/write operation on the 1-byte register, the IIC increments the address by 1 until it reaches 0x11, then returns to 0x00 to continue the next cycle.

10.2 register specification

10.2.1 Ctrl0 register (register 00)

Table 10-2 Overview of Ctrl0 Register

Bit	Symbol	Value	Description
7	EXT_TEST	**0**[*1]	normal mode
		1	external clock test mode
6	-	0	Not used, keep it at 0
5	STOP	**0**	RTC clock working properly
		1	The RTC clock stops working, and the divider below 8.096kHz is set to 0.
4	SR	**0**	regular work
		1	Perform soft reset[*2]
3	-	0	Not used, keep it at 0
2	CIE	**0**	No hardware interrupt is generated during internal calibration
		1	Each internal calibration process generates a hardware interrupt.
1	12_24	**0**	24-hour mode
		1	12-hour mode
0	CAP_SEL	**0**	Adaptation of 7pF Load Crystal Oscillator
		1	Adaptation of 12.5pF Load Crystal Oscillator

*1 The **bold red text** indicates the default power-up value of the corresponding register bit
*2 Send 0x58 to the Ctrl0 register for the system to perform a soft reset

- EXT_TEST

Setting the EXT_TEST bit to 1 activates test mode, where CLKOUT functions as an input pin to receive external clock signals that override the internal 32.768kHz clock for timing. The external clock is divided by 64 to control the second pulse flip. The STOP bit configures the 64-divider's initial state, and setting it to 1 resets the divider to zero.

The external clock frequency must be no less than 1MHz and the high level width must be no less than 300ns.

Test mode example:

1. Set the EXT_TEST bit to 1
2. Set the STOP bit to 1
3. The STOP bit is 0
4. Set the initial value of the RTC register
5. Inject 32 clock pulses through the CLKOUT pin
6. Monitor RTC register flip for 1 second
7. Inject 64 clock pulses through the CLKOUT pin
8. Monitor RTC register flip for 1 second
9. Repeat steps 7 and 8 to monitor the RTC register flip state.

- STOP

The STOP bit enables precise timing control. When set to 1, it resets the high-level flip-flop (F2 to F14) in the clock divider circuit, eliminating the second pulse. This also prevents the CLKOUT pin from generating clock signals below 8.092 kHz.

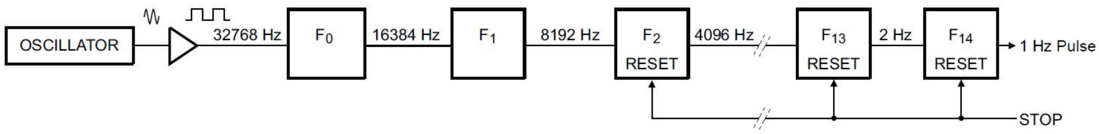


Figure 10-1 STOP Bit Function Block Diagram

When the STOP bit is set to 0, the first second pulse is generated after 0.5s to 0.5s+122μs, followed by one second pulse every second thereafter. The 122μs uncertainty in the timing of the first second pulse arises because the F0 and F1 registers are not controlled by the STOP signal. When the STOP bit is set to 0 via IIC, its state cannot be determined.

- SR

The chip incorporates a power-up reset circuit that resets all registers and state machine upon power-on to ensure normal system operation. In exceptional cases of abnormal chip status, a soft reset command (writing 0x58 to the Ctrl0 register) can be issued to perform a soft reset operation.

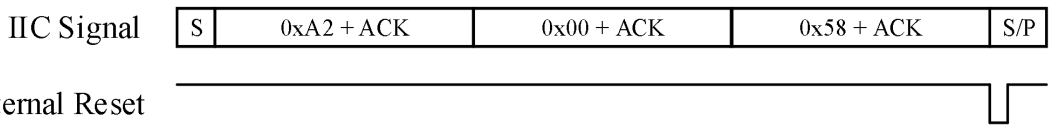


Figure 10-2 Soft reset sequence

If the IIC state machine malfunction prevents sending the soft reset command, the chip's built-in super reset command can be used to reset the chip. The timing sequence of the super reset command is shown in Figure 10-3.

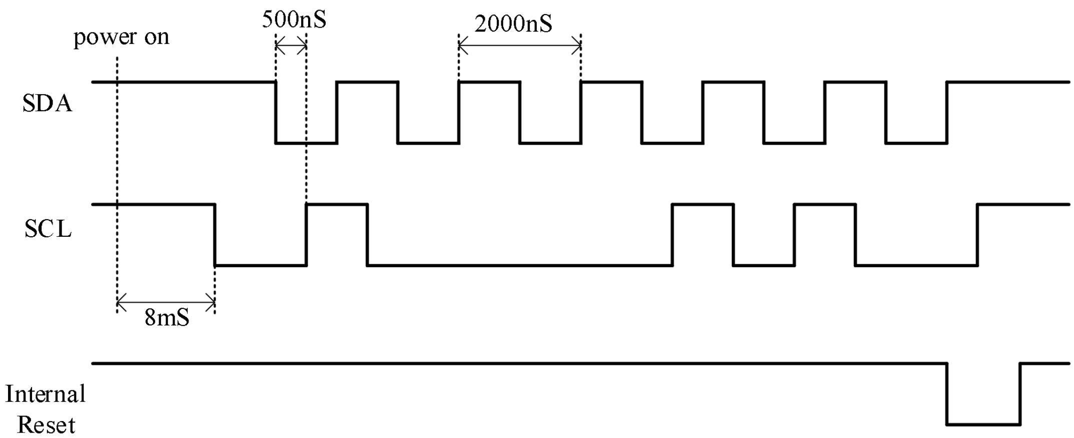


Figure 10-3 Super Reset Sequence

- CIE

Controls whether the internal OFFSET calibration status is output through the INTN interrupt pin. When set to 1, the INTN pin outputs an interrupt signal during each internal calibration process. When set to 0, no interrupt signal is output through the INTN pin.

- 12_24

Set the RTC clock to 12-hour or 24-hour mode.

- CAP_SEL

The JXR2060 supports 32.768kHz crystal oscillators with 7pF or 12.5pF load capacitance, with the CAP_SEL bit controlling the oscillator type selection.

10.2.2 Ctrl1 register (Register 01)

Table 10-3 Overview of Ctrl0 Register

Bit	Symbol	Value	Description
7	AIE	**0**[*1]	No hardware interrupt is generated when an alarm interrupt occurs.
		1	A hardware interrupt is generated when an alarm interrupt occurs.
6	AF	**0**	Read: No alarm interruption occurred
			Write: Clear the alarm interrupt
		1	Read: Alarm interrupt occurred
			Write: Invalid operation
5	MI	**0**	Disable minute timer interrupt
		1	enable minute timer interrupt
4	HMI	**0**	Half-minute timeout is disabled
		1	Enable half-minute timer interrupt
3	TF	**0**	Read: No scheduled interrupt (minute, half-minute, or fixed period)
			Write: Clear scheduled interrupts (minutes, half minutes, or fixed intervals)
		1	Read: Occurs at scheduled intervals (minutes, half minutes, or fixed cycles)
			Write: Invalid operation
2 ~ 0	COF[2:0]	Table 10-5	Control the CLKOUT output clock frequency

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

- AIE

When an alarm interrupt occurs (AF is set to 1 and not cleared), the system determines whether the corresponding hardware interrupt signal will be generated on the interrupt pin based on the AIE status.

- AF

When an alarm interrupt occurs, the AF bit is automatically set to 1 and remains at this level until the user manually resets it to 0 via an IIC command.

- MI & HMI

The minute and half-minute timed interrupts generate interrupt signals synchronized with the second pulse at fixed intervals on the interrupt pin. The interrupt signal format is controlled by TI_TP, with a pulse mode duration of 1/64 second. When configuring these interrupts, ensure the OFFSET adjustment is set to NORMAL MODE.

The minute-level interrupt is triggered at 00:00 every minute, while the half-minute interrupt occurs at both 00:00 and 30:00. These two interrupts operate independently without interference. Figure 10-4 illustrates the interrupt pin outputs when MI is set to 1, and Table 10-4 details the interrupt signal output cycles for different MI and HMI configurations.

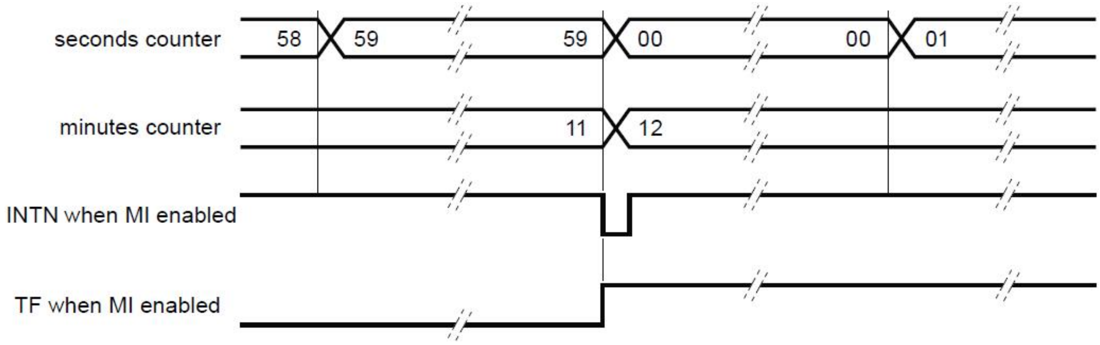


Figure 10-4 Timing sequence of the 4-minute interrupt (pulse mode)

Table 10-4 INTN Signal Description for Different MI and HMI Configurations

MI	HMI	INTN Result
0	0	does not generate interrupt signals
0	1	Generate an interrupt signal every half minute
1	0	Generate an interrupt signal every minute
1	1	Generate an interrupt signal every half minute

The Offset function adjusts the period of minute or half-minute timed interrupts. The interrupt period remains consistent only when all bits in OFFSET[6:0] are set to 0.

- TF

The timer interrupt flag (TF bit) automatically sets to 1 when minute, half-minute, or fixed-period interrupts occur, and remains set until the user manually resets it to 0 via an IIC command.

- COF

COF[2:0] controls the CLKOUT output frequency. The CLKOUT pin operates as a push-pull output, with the frequency output function enabled by default upon power-up. To disable this function, set COF[2:0] to 3'b111 or pull CLKOE low, which will keep CLKOUT low. The STOP bit resets the clock dividers F2 to F14, preventing CLKOUT from generating clock signals below 8.192kHz. Refer to Table 10-5 for detailed CLKOUT output specifications.

Table 10-5 CLKOUT Output Frequency Control

COF[2:0]	CLKOUT output frequency (Hz)	duty cycle	Whether affected by the STOP bit
000[*1]	32768	40% ~ 60%	No effect
001	16384	50%	No effect
010	8192	50%	No effect
011	4096	50%	CLKOUT = 0
100	2048	50%	CLKOUT = 0
101	1024	50%	CLKOUT = 0
110	1[*2]	50%	CLKOUT = 0
111	CLKOUT = 0	-	-

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

*2 The clock frequency accuracy at 1Hz output is affected by the Offset register state

10.2.3 **Offset register (Register 02)**

The JXR2060 features a built-in timing precision adjustment function, enabling calibration of daily timing errors and compensation for oscillator aging or temperature variations.

Table 10-6 Overview of Offset Registers

Bit	Symbol	Value	Description
7	MODE	**0***1	Normal mode, calibration performed every 2 hours
		1	Quick mode, correct every 4 minutes
6 ~ 0	OFFSET[6:0]	Table 10-7	Offset correction value

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

The Offset correction range is-64LSB to +63LSB. In normal mode, the correction precision per LSB is 4.34ppm, while in fast mode, it is 4.069ppm. Refer to Table 10-7 for detailed correction specifications.

Table 10-7 Offset Adjustment Table

OFFSET[6:0]	Offset value (decimal)	Frequency deviation (ppm)	
		MODE = 0	MODE = 1
0111111	+63	+273.420	+256.347
0111110	+62	+269.080	+252.278
...	...	...	...
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000*1	0	**0***1	**0***1
1111111	-1	-4.340	-4.069
1111110	-2	-8.680	-8.138
...	...	...	...
1000001	-63	-273.420	-256.347
1000000	-64	-277.760	-260.416

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

The timing precision correction is implemented by adjusting the count value of the second pulse generator without affecting the output frequency of the crystal oscillator. By setting the CIE bit of the Ctrl0 register to 1, the correction event can be monitored via the interrupt output pin. Each correction event triggers a low-level pulse on the INTN output.

When MODE = 0, the calibration operation is performed every 2 hours. Each calibration step is executed at a specific step count (N), with one step performed between minutes 0 and N-1. In this mode, any clock source or timer in the chip operating below 64Hz will be affected by Offset.

In MODE = 1, the calibration operation executes every 4 minutes, with one step performed per second. If the step count exceeds 60, the excess operations are concentrated in the 59th second. The fast calibration mode provides more accurate clock signals but consumes more power. In this mode, clocks below 1024Hz used as clock sources or timers in the chip are affected by Offset.

Table 10-8 Time Correction Execution Table

	MODE = 0			MODE = 1		
adjusted value	Calibration time	carry out	Number of INTN interrupts per minute *1	Calibration time	carry out	Number of INTN interrupts per second *2
±1	2h	00 min	1	4min	00 sec	1
±2	2h	00 & 01 min	1	4min	00 & 01 sec	1
±3	2h	00 ~ 02 min	1	4min	00 ~ 02 sec	1
…	…	…	…	…	…	…
±59	2h	00 ~ 58 min	1	4min	00 ~ 58 sec	1
±60	2h	00 ~ 59 min	1	4min	00 ~ 59 sec	1
±61	2h	00 ~ 59 min	1	4min	00 ~ 58 sec	1
	2 hours + next hour	00 min	1	4min	59 sec	2
±62	2h	00 ~ 59 min	1	4min	00 ~ 58 sec	1
	2 hours + next hour	00 & 01 min	1	4min	59 sec	3
±63	2h	00 ~ 59 min	1	4min	00 ~ 58 sec	1
	2 hours + next hour	00 ~ 02 min	1	4min	59 sec	4
-64	2h	00 ~ 59 min	1	4min	00 ~ 58 sec	1
	2 hours + next hour	00 ~ 03 min	1	4min	59 sec	5

*1 MODE = 0: The interrupt signal width on the INTN pin is 1/64 second

*2 MODE = 1: the interrupt signal width on the INTN pin is 1/1024 second. For cases where multiple interrupts occur within 1 second, the pulse interval is 1/512 second

Table 10-9 Effect of Offset on Frequency

frequency (Hz)	The Influence of Offset on Frequency	
	MODE = 0	MODE = 1
CLKOUT		
32768	No effect	No effect
16384	No effect	No effect
8192	No effect	No effect
4096	No effect	No effect
2048	No effect	No effect
1024	No effect	No effect
1	be affected	be affected
fixed period interrupt clock source		
4096	No effect	No effect
64	No effect	be affected
1	be affected	be affected
1/60	be affected	be affected

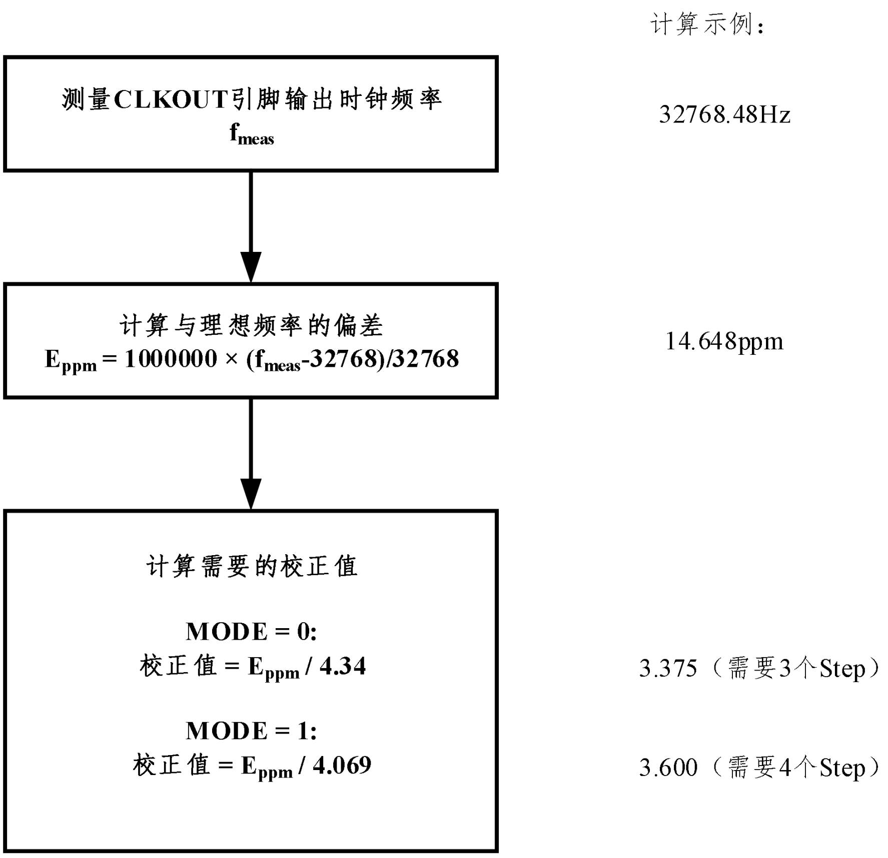


Figure 10-5 Calibration Process Example

10.2.4 RAM register (Register 03)

The JXR2060 provides a byte-sized user RAM for storing system status data and other information.

Table 10-10 RAM Register Overview

Bit	Symbol	Value	Description
7 ~ 0	B[7:0]	**00000000**[*1] ~ **11111111**	Offset correction value

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

10.2.5 Clock & Calendar registers (registers 04 to 0A)

- OS

The OS flag indicates oscillator stoppage. During power-up, the crystal oscillator requires time to stabilize, so the OS flag defaults to 1. After stabilization, users can reset it to 0 via IIC commands. If the oscillator stops abnormally during operation, the OS flag remains set. It stays active until manually reset to 0. This flag alerts users to an oscillator stoppage, requiring RTC clock reset.

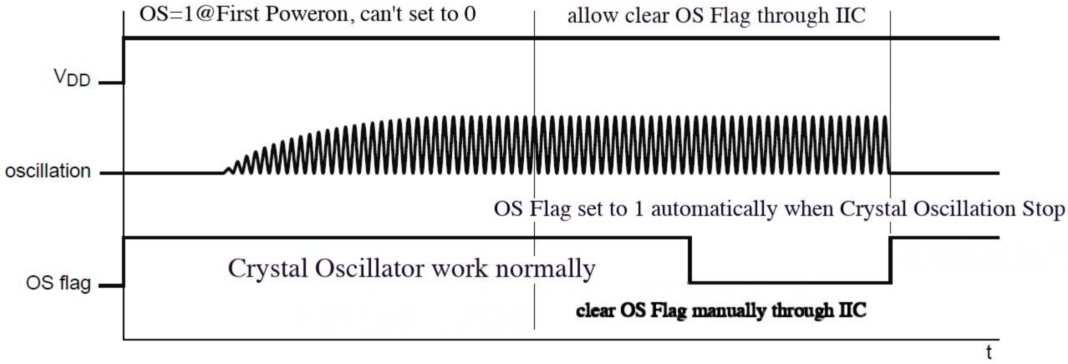


Figure 10-6 OS Flag Status Example

- AMPM

12-hour timekeeping: A 0 in this bit indicates morning, while a 1 indicates afternoon.

24-hour timer: This bit is the most significant bit of the hour count.

- Data format

All data except the carry register (register 08) are in BCD code format. For example, the sub-register value 8'b0101 1001 indicates the current time is 59 minutes.

- Year Register and Leap Year

The year register's value ranges from 00 to 99, resetting to 00 after 99. A year is considered a leap year if its value is divisible by 4. The calendar's validity period spans from 2000 to 2099.

- address register

The address register has three valid bits (bit2 to bit0), with their specific mappings shown in Table 10-11 below.

Table 10-11 Week Register Correspondence Table

bit2	bit1	bit0	week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	**1**	**0**	Saturday*1

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

- register read and write

When operating the read/write clock and calendar register, the internal clock counter is frozen to prevent carry generation during read/write operations, which could affect time accuracy. After the read/write operation completes, the internal counter resumes and supplements the carry operations during the read/write process.

The clock counter can only record one carry operation, so the read and write operations of the clock and calendar registers must be completed within 1 second, otherwise seconds will be lost.

For these reasons, we recommend that users perform all clock and calendar register (registers 04 to 0A) read/write operations in a single IIC operation to prevent carry-related errors between consecutive IIC operations.

10.2.6 Alarm register (registers 0B to 0F)

Alarm interrupts can be configured flexibly to occur at specific times, such as X hour X minute X second weekly or X day X hour X minute X second monthly. Each alarm register contains an AEN_X (bit7) bit. When the AEN_X bit of a particular alarm register is 0, its set value must be compared with the corresponding clock register value; if they match, an alarm interrupt is triggered. If the AEN_X bit is 1, the corresponding alarm register value is ignored, meaning no comparison with the clock register is required, and the register value is always considered consistent with the clock register value. During an alarm interrupt, the AF bit is set to 1. If AIE = 1, a hardware interrupt signal synchronized with AF is simultaneously generated on the INTN pin.

Table 10-12 Alarm Interrupt Settings

AEN_W	AEN_D	AEN_H	AEN_M	AEN_S	alarm interrupt
1	1	1	1	1	no alarm interrupt generated
1	1	1	1	0	SEC second alarm per minute per hour per day
1	1	1	0	1	Daily hourly MIN: 00 alarm
1	1	1	0	0	Daily hourly MIN: SEC alarm
1	1	0	1	1	Alarm every hour at 00:00
1	1	0	1	0	Daily HOUR-hour-minute-SEC-second alarm
1	1	0	0	1	Daily HOUR: MIN: 00 Alarm
1	1	0	0	0	Daily HOUR: MIN: SEC Alarm
1	0	1	1	1	Alarm at 00:00:00 every DAY
1	0	1	1	0	SEC alarm for every day, every hour, every minute
1	0	1	0	1	Alarm at 00:00 every DAY
1	0	1	0	0	DAY DAY hour MIN:SEC alarm
1	0	0	1	1	Alarm triggered at DAY:00:00
1	0	0	1	0	Alarm triggered by DAY, HOUR, MINUTE, and SEC
1	0	0	0	1	Alarm: DAY: HOUR: MIN: 00
1	0	0	0	0	Alarm: DAY: HOUR: MIN: SEC
0	1	1	1	1	Weekly 00:00:00 alarm
0	1	1	1	0	Weekly, hourly, and minute-by-minute SEC second-level alarms
0	1	1	0	1	Weekly MIN: 00 alarm
0	1	1	0	0	Weekly MIN:SEC alarm
0	1	0	1	1	WEEK's HOUR: 00:00 Alarm
0	1	0	1	0	Weekly Hourly Minute-by-Minute Second-by-Second Alarm
0	1	0	0	1	Weekly Hour: Alarm at 00:00
0	1	0	0	0	Weekly Hour: Minute: Second Alarm
0	0	1	1	1	00:00:00 alarm for WEEK and DAY
0	0	1	1	0	Hourly and minute-by-minute alarms for both WEEK and DAY
0	0	1	0	1	Hourly MIN:00 alarm for WEEK and DAY
0	0	1	0	0	WEEK and DAY alarms with hourly MIN:SEC settings
0	0	0	1	1	WEEK and DAY hour: 00:00 alarm
0	0	0	1	0	Alarm triggered by weekly (WEEK) and daily (DAY) cycles, hourly (HOUR), minute-by-minute (MIN), and second-by-second (SEC) intervals
0	0	0	0	1	WEEK and DAY HOURS: MIN: 00 Alarm
0	0	0	0	0	Alarm for WEEK and DAY, with HOURS, MINUTES, and SECS:

10.2.7 Timer registers (registers 10,11)

Table 10-13 Timer value register overview

Bit	Symbol	Value	Description
7 ~ 0	T[7:0]	**00000000**[*1] ~ **11111111**	Fixed cycle interrupt count[*2]

*1 The **bold red text** indicates the default power-up value of the corresponding register bit
*2 The fixed period value is calculated as T divided by SourceClockFrequency (where T is the countdown value)

Table 10-14 Timer mode register overview

Bit	Symbol	Value	Description
7 ~ 5	-	**000**[*1]	Not used, keep it at 0
4 ~ 3	TCF[1:0]	00	The clock source for the countdown is 4096Hz.
		01	The countdown clock source is 64Hz
		10	The countdown clock source is set to 1Hz
		11[*1]	The clock source of the countdown is 1/60 Hz.
2	TE	**0**[*1]	Disable the counter
		1	enable counter
1	TIE	**0**[*1]	Fixed-period interrupts do not generate hardware interrupts
		1	Generate a hardware interrupt when a fixed-period interrupt occurs
0	TI_TP	**0**[*1]	The hardware interrupt is in continuous mode, following the interrupt flag.
		1	Hardware interrupt in pulse mode

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

- T

The IIC instruction allows configuration of T[7:0] as the countdown value for fixed-period interrupts. Valid data ranges from 1 to 255, and setting it to 0 terminates the interrupt. When the countdown reaches 1, the interrupt flag TF is set to 1, T[7:0] resets to its initial value, and the next countdown cycle begins.

- TCF

Controls the clock source for fixed-period interrupt countdown. By selecting different clock sources and setting various countdown values, it flexibly supports fixed-period interrupt functions ranging from 244μs to 4 hours and 15 minutes. When the fixed-period interrupt function is not in use, TCF[1:0] should be set to 2'b11 to reduce current power consumption.

Table 10-15 Fixed Period Interrupt Clock Source and Period Settings

TCF[1:0]	countdown clock source	interrupt cycle		Pulse mode (TI_TP = 1) interrupt signal width	
		Minimum period (T = 1)	Maximum period (T = 255)	T = 1	T > 1
00	4096Hz	244μs	62.256ms	1/8192	1/4096
01	64Hz	15.625ms	3.984s	1/128	1/64
10	1Hz*1	1s	255s	1/64	1/64
11	1/60Hz*1	60s	4h15m	1/64	1/64

*1 The timing precision calibration operation (offset register-related) affects the clock source period

- TE

The countdown timer enable bit: When set to 0, the timer is disabled; when set to 1, the timer is enabled and starts counting down at the clock frequency specified by TCF[1:0].

- TIE

In the state of fixed period interrupt, according to the state of TIE, determine whether the corresponding hardware interrupt signal will be generated on the interrupt pin.

- TI_TP

The hardware output configuration for timing interrupts (including fixed-period, minute, and half-minute interrupts) is determined by TI_TP. When TI_TP is set to 0, the interrupt output operates in continuous mode, with the interrupt waveform following the TF bit. The hardware interrupt signal must be cleared by the user through IIC commands to reset the TF flag. When TI_TP is set to 1, the interrupt output operates in pulse mode, generating a fixed-length INTN low pulse for each interrupt event.

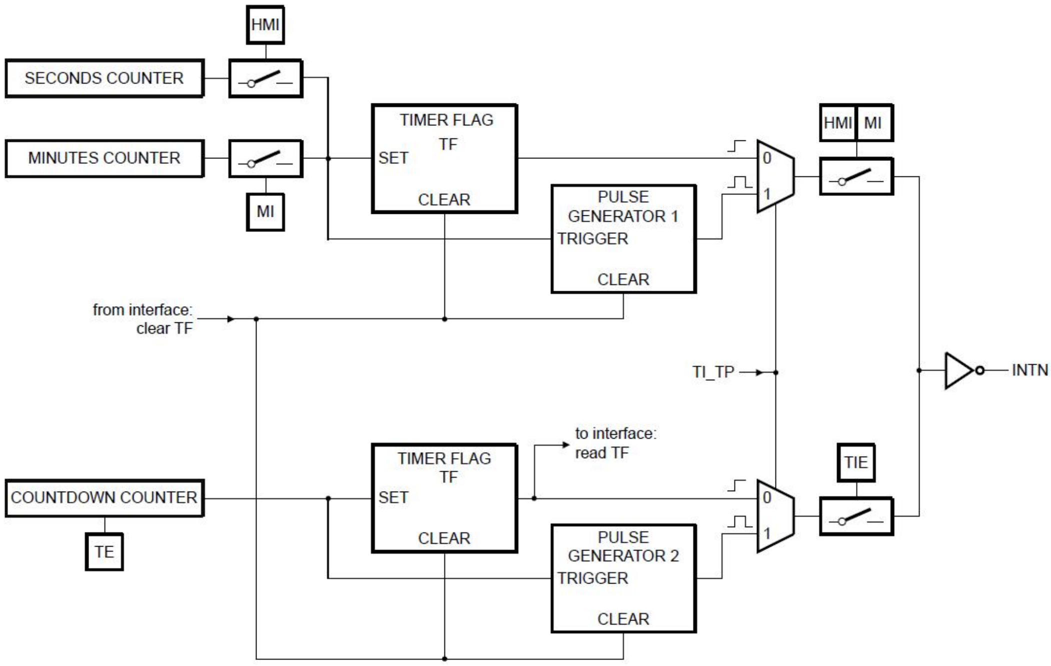


Figure 10-7 Timing Interrupt Structure Diagram

10.2.8 **Set register (Register 12)**

Table 10-16 Overview of Setting Registers

Bit	Symbol	Value	Description	
7	-	**0***1	Not used, keep it at 0	
6 ~ 3	-	**0000***1	Can be used as RAM	
2	DET_EN	0	Disable stoppage detection	
		1*1	Enable stop-motion detection	
1 ~ 0	ADJ[1:0]	00	By default, the system supports driving an ESR 150kΩ crystal oscillator. For external oscillators with lower ESR values, adjusting the ADJ setting can reduce the chip's total current power consumption (the table on the right shows the chip's total current power consumption at different ADJ settings).	800nA
		01		700nA
		10*1		**600nA**
		11		500nA

*1 The **bold red text** indicates the default power-up value of the corresponding register bit

11 interrupt capability

11.1 alarm interrupt

Alarm interrupts can be triggered at specified days, hours, minutes, or seconds.

11.1.1 alarm interrupt timing

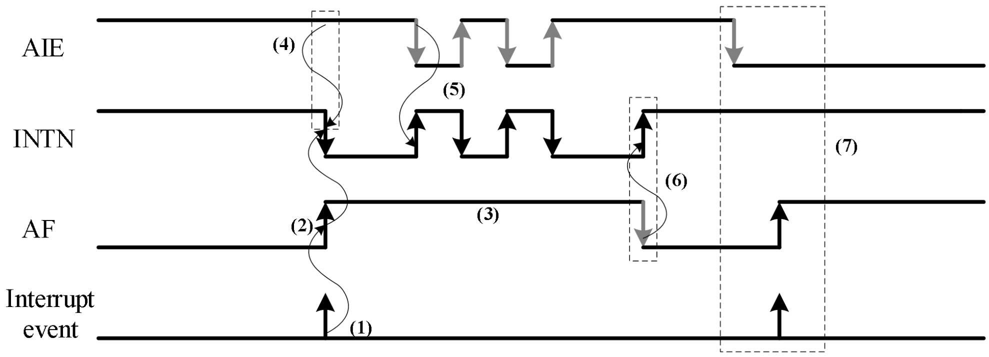


Figure 11-1 Alarm Interrupt Sequence

(1) Configure the alarm interrupt with specified hour, minute, second, date, and day of the week, along with the AEN_X register. The alarm interrupt is triggered when the set time matches the current time.

(2) When an alarm interrupt occurs, the AF flag is set to 1.

(3) The AF register remains at 1 until manually cleared to 0.

(4) When an alarm interrupt occurs, INTN outputs low level if AIE equals 1, and remains high-impedance if AIE equals 0.

(5) When INTN = 0, setting AIE to 0 immediately restores INTN to high-impedance state. AIE can control INTN's output state until the alarm interrupt event occurs and the AF register is cleared to 0.

(6) Clearing the AF register to 0 deactivates the alarm interrupt output, causing INTN to immediately transition from low to high impedance.

(7) When an alarm interrupt occurs, if AIE equals 0, INTN remains in a high-impedance state and does not output a low level, but the AF flag is set to 1.

11.1.2 alarm interrupt related register

Table 11-1 Alarm Interrupt Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control and Status registers										
01	Ctrl1	8′ h00	**AIE**	**AF**	MI	HMI	TF	COF[2:0]		
Alarm registers										
0B	SEC Alarm	8′ h80	**AEN_S**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
0C	MIN Alarm	8′ h80	**AEN_M**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
0D	HOUR Alarm	8′ h80	**AEN_H**	○	**20**	**10**	**8**	**4**	**2**	**1**
				○	**AM/PM**	**10**	**8**	**4**	**2**	**1**
0E	DAY Alarm	8′ h80	**AEN_D**	○	**20**	**10**	**8**	**4**	**2**	**1**
0F	WEEK Alarm	8′ h80	**AEN_W**	○	○	○	○	**4**	**2**	**1**

- When configuring the alarm interrupt register, it is recommended to first set AIE to 0 to prevent unnecessary hardware interrupts during operation.
- An alarm interrupt event sets the AF flag at position 1, which remains at 1 until manually cleared to 0 via the IIC port.
- When an alarm interrupt occurs, the AIE determines whether to generate an interrupt signal output (if AIE = 1, INTN = 0; if AIE = 0, INTN = Hi-Z).
- AEN_X bit 0 indicates that the alarm register must be compared with the corresponding clock register. If AEN_X bit 1 is set, the alarm register is not compared with the corresponding clock register, meaning it is always considered to match the clock register. Refer to Table 10-12 for the specific correspondence.

11.2 fixed periodic interrupt

The fixed period interrupt can produce interrupt events between 244μS and 4h15m according to a set period.

11.2.1 fixed period interrupt timing

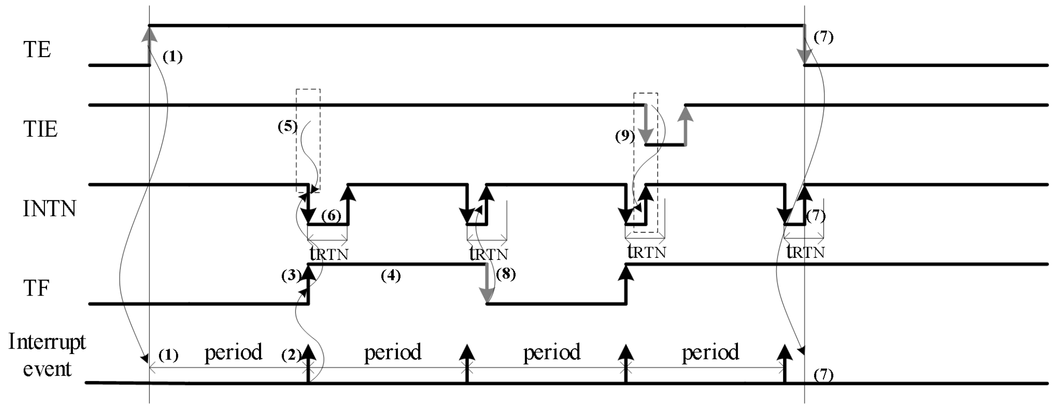


Figure 11-2 Fixed Period Interrupt Timing (TI_TP = 1)

(1) When the TE bit is set to 1, the fixed-period counter starts counting down from its preset value.

(2) An interrupt event occurs when the counter counts down from 01h to 00h. The counter 0x10 resets to its preset value and continues the next countdown.

(3) When a fixed-period interrupt occurs, the TF register is set to 1.

(4) The TF register remains at 1 until manually cleared to 0 via the IIC port.

(5) When a fixed-period interrupt event occurs, INTN outputs a low level if TIE = 1, and remains high-impedance if TIE = 0.

(6) The INTN output remains low for tRTN duration before automatically reverting to high-impedance state until the next interrupt signal is triggered. The tRTN value is specified in Table 10-15.

(7) When the TE bit is set to 0, the counter stops counting and ceases generating fixed-period interrupts. The INTN output enters a high-impedance state (if the TE bit is set to 0 during an INTN = 0 period, the INTN immediately returns to high-impedance state).

(8) If TF is cleared to 0 during the INTN = 0 period, INTN immediately resumes the high-resistance state.

(9) When TIE writes 0, INTN immediately returns to high-impedance state.

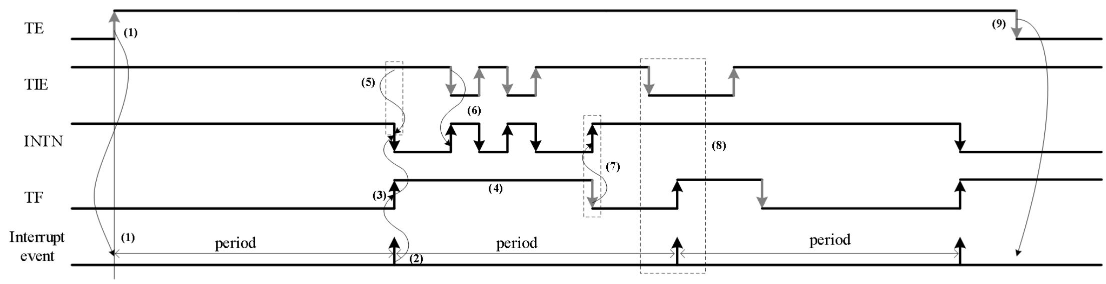


Figure 11-3 Fixed Period Interrupt Timing (TI_TP = 0)

(1) When the TE bit is set to 1, the fixed-period counter starts counting down from its preset value.

(2) An interrupt event occurs when the counter counts down from 01h to 00h. The counter 0x10 resets to its preset value and continues the next countdown.

(3) When a timer interrupt occurs, the TF flag is set to 1.

(4) The TF register remains at 1 until manually cleared to 0 via the IIC port.

(5) When a fixed-period interrupt event occurs, if TIE = 1, INTN outputs a low level; if TIE = 0, INTN remains in a high-impedance state.

(6) When INTN = 0, setting TIE to 0 immediately restores INTN to high-impedance state. TIE controls INTN's output state until the fixed-period interrupt occurs and TF register is cleared to 0.

(7) Clearing the TF register to 0 disables the timer interrupt output, and INTN immediately transitions from 0 to high impedance.

(8) When a fixed-period interrupt occurs, if TIE = 0, INTN remains in a high-impedance state and does not output a low level, but the TF flag is set to 1.

(9) Setting TE to 0 during INTN = 0 does not clear the interrupt status, and no new interrupt events will occur.

11.2.2 fixed period interrupt related register

Table 11-2 Fixed Period Interrupt-Related Registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control and Status registers										
01	Ctrl1	8′ h00	AIE	AF	MI	HMI	**TF**	**COF[2:0]**		
Timer registers										
10	Timer Value	8′ h00	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
11	Timer Mode	8′ h18	○	○	○	**TCF[1:0]**		**TE**	**TIE**	**TI_TP**

- When configuring fixed-period interrupt registers, it is recommended to first set both TE and TIE to 0 to prevent unnecessary hardware interrupts during operation.
- TI_TP controls the output format of INTN after a fixed-period interrupt is generated. When TI_TP is set to 0, INTN continuously outputs interrupt alarm signals during the TF and TIE periods. When TI_TP is set to 1, INTN outputs interrupt alarm signals in pulse form, with the specific low pulse width referenced in Table 10-15.
- TCF[1] and TCF[0] are used to set the timer clock frequency. In pulse mode, the automatic reset time tRTN of the interrupt signal on the INTN pin is determined by the timer clock frequency.
- Register 10 sets the counter value (01h to FFh). The counter counts down to 00h at the TCF-defined interval, triggering a fixed-period interrupt event.
- TE is the enable control bit of the fixed-period counter. When TE = 1, the counter starts counting down; when TE = 0, the counter stops counting, terminating the fixed-period interrupt function.
- The occurrence of periodic cycle interrupt events sets the TF flag at position 1, which remains at 1 until manually cleared to 0 via the IIC port.
- When a fixed-period interrupt event occurs, the TIE determines whether to generate a hardware interrupt signal.

11.3 Minute/Quarter-minute timer interrupt

The minute and half minute interrupt can produce fixed period interrupt signal with period of 60s or 30s.

11.3.1 Minute/Quarter-minute timed interrupt sequence

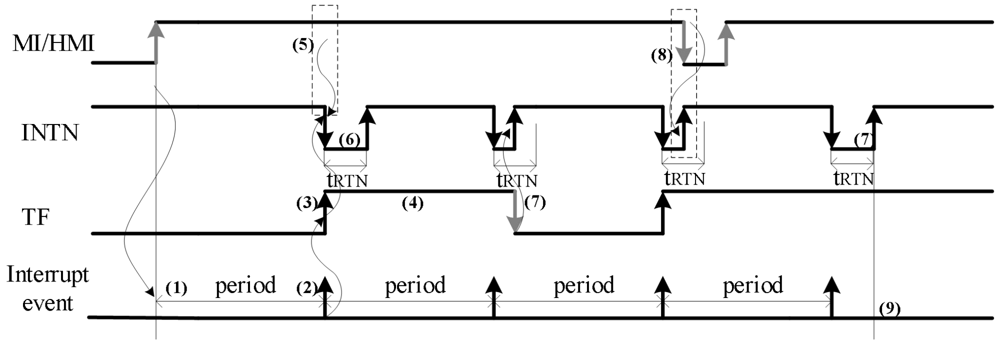


Figure 11-4 minute/half-minute timed interrupt sequence (TI_TP = 1)

(1) An interrupt event is triggered when the MI bit is set to 1, with updates occurring every minute. When the HMI bit is set to 1 and the second register is at 0s/30s, an interrupt event is generated.

(2) Since MI/HMI writes are not synchronized with the internal clock, the first interrupt cycle may be unpredictable, while subsequent interrupt cycles are fixed.

(3) When a timer interrupt occurs, the TF register is set to 1.

(4) The TF register remains at 1 until manually cleared to 0 via the IIC port.

(5) The INTN output goes low when a timer interrupt occurs.

(6) The INTN output remains low for tRTN duration before automatically returning to high-impedance state until the next interrupt signal is triggered. The fixed tRTN value is 1/64 second.

(7) If TF is cleared to 0 during the INTN = 0 period, INTN immediately resumes the high-resistance state.

(8) Set MI/HMI to 0 during the INTN = 0 period, and immediately restore the high-resistance state of INTN.

(9) MI/HMI value of 0 between two interrupt events does not affect the interrupt cycle.

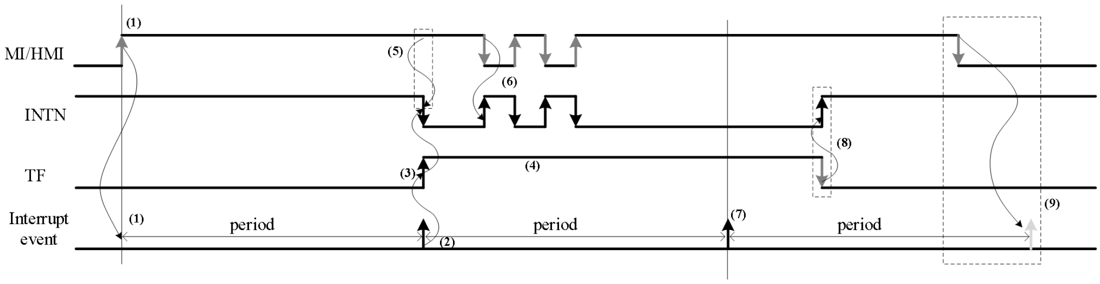


Figure 11-5 minute/half-minute timed interrupt sequence (TI_TP = 0)

(1) An interrupt event is triggered when the MI bit is set to 1, with updates occurring every minute. When the HMI bit is set to 1 and the second register is at 0s/30s, an interrupt event is generated.

(2) Since MI/HMI writes are not synchronized with the internal clock, the first interrupt cycle may be unpredictable, while subsequent interrupt cycles are fixed.

(3) When a timer interrupt occurs, the TF register is set to 1.

(4) The TF register remains at 1 until manually cleared to 0 via the IIC port.

(5) The INTN output goes low when a timer interrupt occurs.

(6) If MI/HMI is set to 0 during INTN = 0, INTN immediately returns to high-impedance state. MI/HMI can control INTN's output state until the minute/half-minute timer interrupt event occurs and TF register is cleared to 0.

(7) If the TF is not cleared to 0 after an interrupt event, the INTN and TF states will remain unchanged during subsequent interrupt events, making it impossible to detect the occurrence of a scheduled interrupt.

(8) Clear TF to 0 during INTN = 0, and INTN immediately resumes the high-resistance state

(9) After setting MI/HMI to 0, minute/quarter-minute timed interrupt events will no longer be generated.

11.3.2 min/half-minute timer interrupt register

Table 11-3 minute/half-minute timer interrupt related registers

Address	Function	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control and Status registers										
01	Ctrl1	8′ h00	AIE	AF	**MI**	**HMI**	**TF**	COF[2:0]		
Timer registers										
11	Timer Mode	8′ h18	○	○	○	TCF[1:0]		TE	TIE	**TI_TP**

- Set MI to 1 and wait 1 to 59 seconds to generate the first interrupt event. Set HMI to 1 and wait 1 to 29 seconds to generate the first interrupt event. Subsequent interrupt events are spaced at 1 minute or 30 seconds.
- TI_TP controls the output format of INTN after minute/quarter-minute timed interrupts. When TI_TP is set to 0, INTN continuously outputs interrupt alarm signals during TF and MI/HMI being active. When TI_TP is set to 1, INTN outputs pulse-form interrupt alarm signals with a fixed low pulse width of 1/64s.
- When a minute/half-minute timed interrupt event occurs, it sets the TF flag to 1, which remains at 1 until manually cleared to 0 via the IIC port.

12 IIC BI

12.1 Characteristics of IIC Bus

The IIC is a bidirectional communication interface where the signal line (SDA) and clock line (SCL) require pull-up resistors to maintain high voltage. The IIC bus port must adopt an open-drain configuration to enable multi-device wiring and connectivity.

12.2 data transmission

Each SCL clock cycle transmits 1bit of data. During transmission, data on the SDA line changes when the SCL is low; during reception, stable and valid data is retrieved from the SDA line when the SCL is high.

12.3 Start and Stop conditions

In idle state, both SCL and SDA remain at high level. During the high-level state of SCL, the falling edge of SDA serves as the initialization signal for IIC communication, while the rising edge of SDA acts as the termination signal for IIC communication.

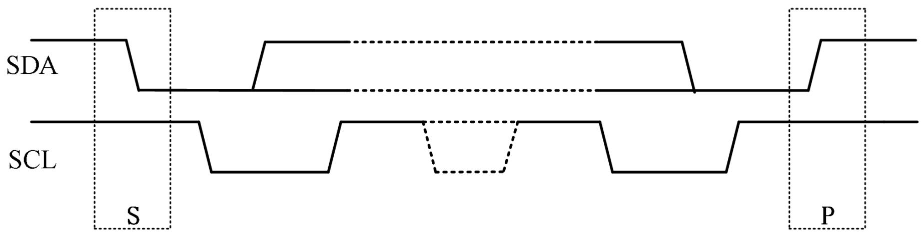


Figure 12-1 start and stop conditions of IIC

12.4 Select device (slave address)

The IIC bus lacks a chip select signal. The master device selects a slave device by sending a unique fixed device number (slave address), and the selected slave device responds to establish communication with the master.

The address consists of 7 bits of data, with 4 bits (Group 1) and 3 bits (Group 2). The slave address of the JXR2060 is "1010001". During communication, the slave address and read/write selection bit are transmitted as 8-bit data.

Slave address							R/W bit
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	0	0	1	R/W

0: write mode
1: read mode

Figure 12-2 IIC Address Schematic

12.5 system configuration

The device that controls the data transmission is called the master device, the device controlled by the master device is called the slave device, the device that sends the data is called the sender, the device that receives the data is called the receiver.

In the JXR2060 system, the CPU or other control devices act as master devices, while the JXR2060 chip itself serves as a slave device. Both master and slave devices can function as either the transmitter or the receiver.

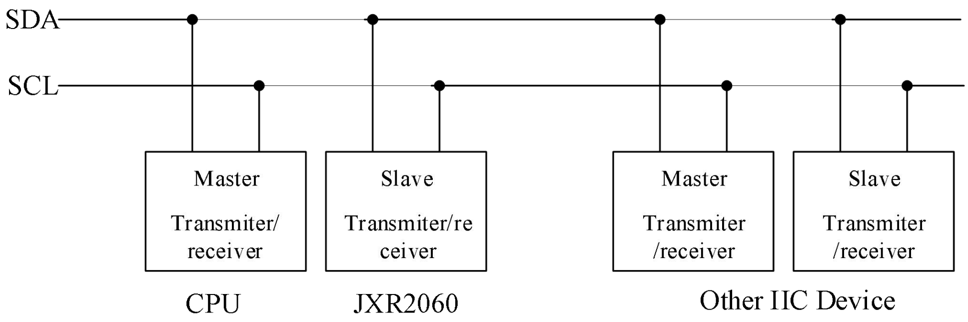


Figure 12-3 IIC System Configuration

12.6 Acknowledge signal

The IIC bus imposes no restrictions on the number of bytes transmitted between start and stop conditions. Upon completion of each byte transfer, the transmitter must release the SDA bus and provide one SCL clock to receive the acknowledge signal. If the receiver successfully receives 8-bit data, it must set the SDA to 0 after the clock cycle of the final 1-bit data transmission. The transmitter then interprets this low level as the successful acknowledge signal. One clock cycle later, the receiver releases the SDA bus and prepares to receive new data.

The IIC bus terminates data transmission when the following conditions are met:

(1) When the master device acts as the transmitter, it terminates the transmission upon receiving the acknowledge signal from the slave device.

(2) When the main device acts as the receiver, it sends a 1 as the acknowledge signal and immediately transmits the stop bit after successfully receiving the 8-bit data.

12.7 IIC bus control

This section describes the IIC bus communication timing when the CPU is the master device and the JXR2060 is the slave device.

12.7.1 addressed write operation

The JXR2060 features an auto-increment address system. Once the target address is set, it simply requires continuous data transmission. The address bits increment automatically, progressing from 0x00 to 0x10, with each increment represented by a bit (0x01,0x02,..., 0x11).

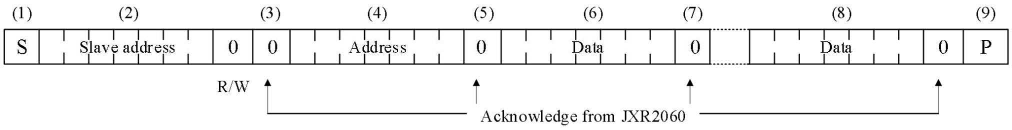


Figure 12-4 specifies the address write operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR2060 slave address and sets it to write mode through the read/write bit.

(3) JXR2060 sends the acknowledge signals.

(4) The CPU sends the write register address to JXR2060.

(5) JXR2060 sends the acknowledge signal.

(6) The CPU sends data to the register at the specified address in (4).

(7) JXR2060 sends the acknowledge signals.

(8) Repeat steps (6) and (7), where the address for writing to the register in JXR2060 will increment automatically.

(9) The CPU sends the stop bit [P].

12.7.2 addressed read operation

After writing to the register, the CPU can read the register data by setting the read mode.

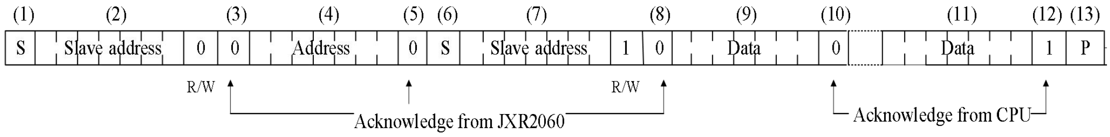


Figure 12-5 Specified Address Read Operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR2060 slave address and sets it to write mode through the read/write bit.

(3) JXR2060 sends the acknowledge signal.

(4) The CPU sends the read register address to JXR2060.

(5) JXR2060 sends the acknowledge signal.

(6) The CPU sends the restart bit.

(7) The CPU sends the JXR2060 slave address and sets it to read mode through the read/write bit.

(8) The JXR2060 sends the acknowledge signal, then the CPU acting as the receiver and the JXR2060 as the transmitter.

(9) The data in the register corresponding to the specified address in JXR2060 Send (4).

(10) The CPU sends the acknowledge signal to JXR2060.

(11) Repeat steps (9) and (10), where the address of the read register in JXR2060 will increment automatically.

(12) The CPU sends No acknowledge signal to JXR2060.

(13) The CPU sends the stop bit [P].

12.7.3 Unspecified address read operation

The master device can directly enter read mode to access the register contents of the slave device. As the master device does not specify the read operation address, the slave device starts reading from the address one unit higher than the previous IIC operation address.

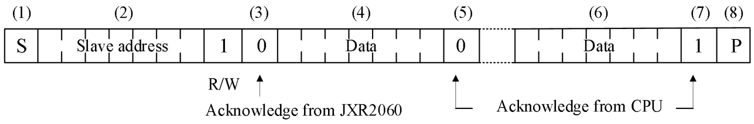


Figure 12-6 Unspecified address read operation

(1) The CPU sends the start bit [S].

(2) The CPU sends the JXR2060 slave address and sets it to read mode through the read/write bit.

(3) The JXR2060 sends the acknowledge signal, with the CPU acting as the receiver and the JXR2060 as the transmitter.

(4) JXR2060 automatically increments the register address and sends the register data.

(5) The CPU sends the acknowledge signal to JXR2060.

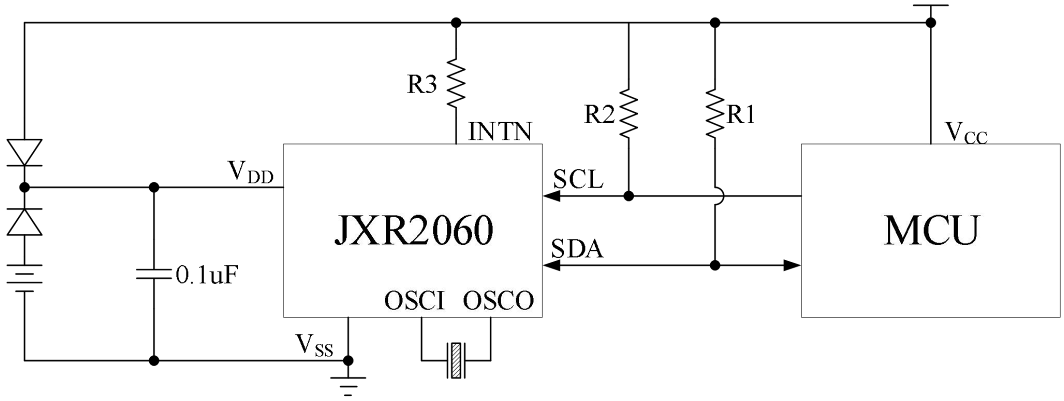
(6) When repeating steps (4) and (5), the address of the read register in JXR2060 will increment automatically.

(7) The CPU sends No acknowledge signal to JXR2060.

(8) The CPU sends the stop bit [P].

Appendix

Example

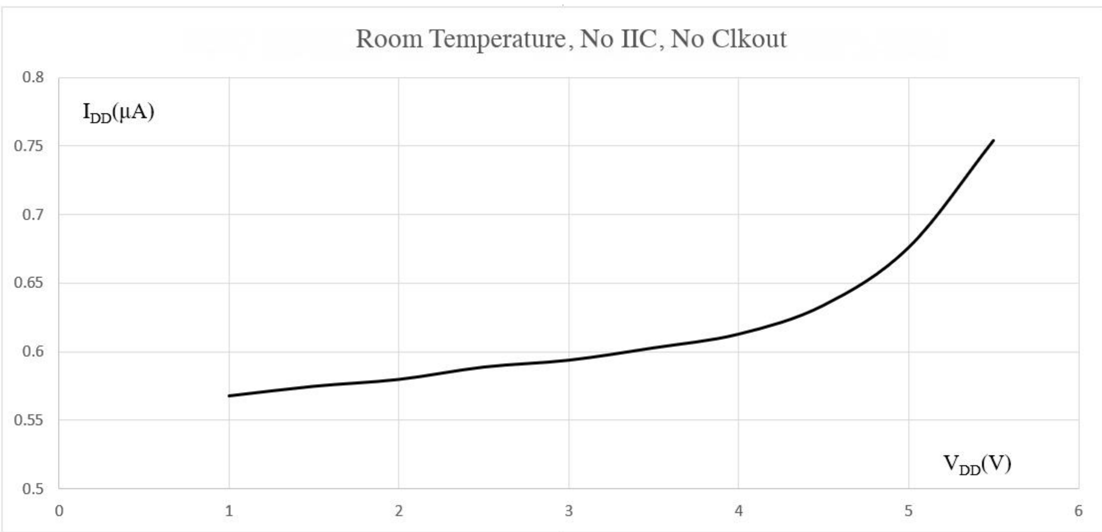


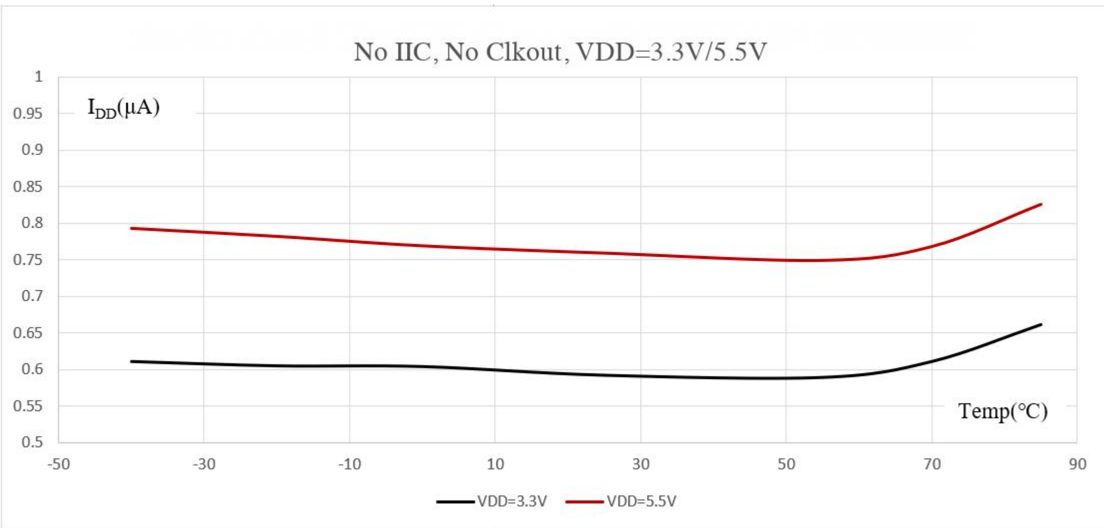
- The IIC pull-up resistor value should be determined based on the actual communication rate. Empirical data shows that when R1 and R2 are 10kΩ, a 100kHz IIC communication rate can be achieved; when R1 and R2 are 4.7kΩ, a 400kHz IIC communication rate can be achieved.
- The INTN is an N-Ch open-drain structure, requiring an external pull-up resistor R3 for measuring interrupt outputs.
- The R3 value should not be excessively high to prevent weak pull-up from causing high-level spikes in INTN output, which may lead to timing errors. A pull-up resistor of approximately 10kΩ is recommended.
- To prevent unnecessary power fluctuations from affecting chip performance, a decoupling capacitor of at least 0.1μF should be added to the chip's power pin (Pin8). The capacitance value may vary depending on the application environment, but it must ensure the power fluctuations remain within a safe range.
- When using non-rechargeable batteries as backup power for dual-supply systems, an isolation diode must be added to prevent reverse current flow.

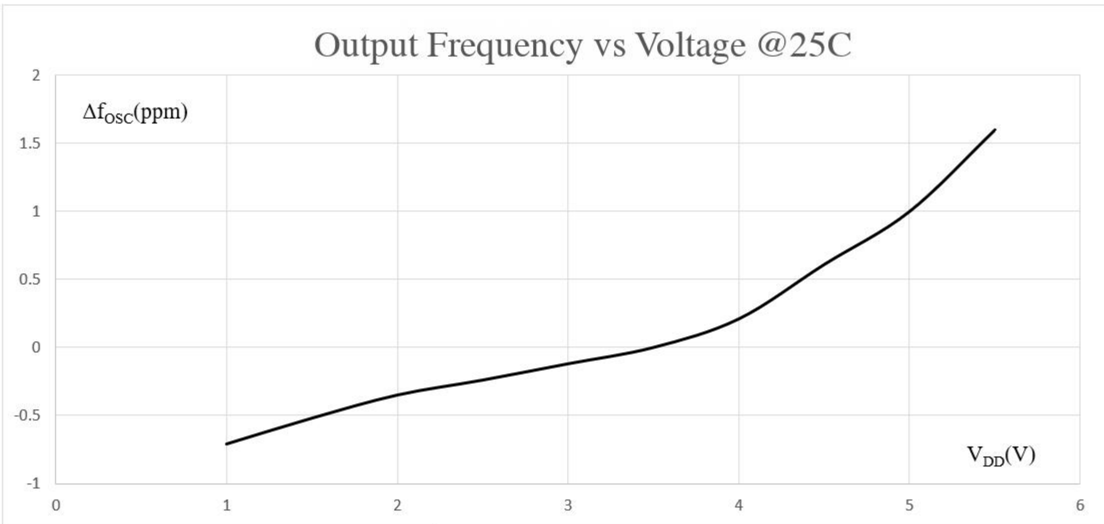
direction for use

- The product features an electrostatic protection rating of HBM ±2.0kV and CDM ±1.0kV. During operation, precautions must be taken to prevent electrostatic discharge.
- During operation, power spikes exceeding 8.25V may trigger latch-up effects and circuit damage. To ensure stable chip operation, install a decoupling capacitor (minimum 0.1uF) near the clock chip's power pin.
- Because the clock chip is a low power integrated circuit product, it is necessary to avoid placing any high noise components around the clock chip.
- Leaving the chip's input pins floating may increase current power consumption. During operation, these pins should be connected to a fixed potential (VDD or VSS).
- The chip's humidity sensitivity level is Level 3. From unpacking to soldering onto the board, the workshop storage environment must maintain a temperature and humidity of no more than 30°C and 60% RH, respectively, with a storage duration not exceeding 168 hours. If these storage conditions are exceeded, the chip must undergo baking treatment before SMT mounting, with baking conditions set at 125°C for 16 hours or 60°C for 48 hours.

measured data







timing accuracy

The temperature-dependent output frequency of a clock chip can be calculated using the following formula:

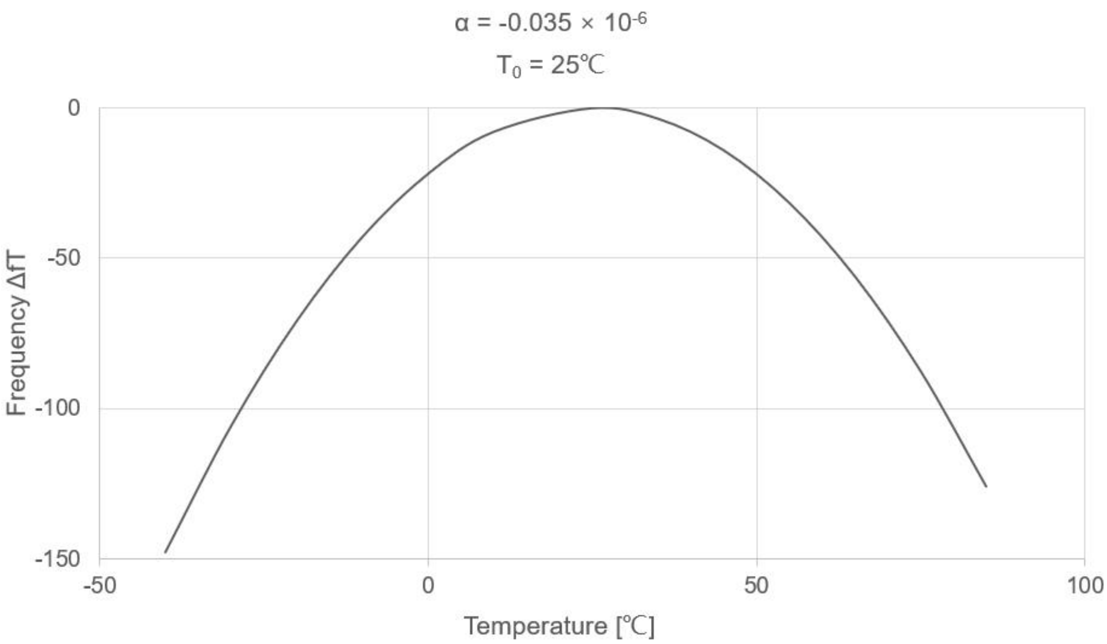
$$\Delta fT = \alpha\left(T - T_0\right)^2$$

ΔfT ΔfT frequency temperature deviation

$\alpha\left[1/^{\circ}C^2\right]$ $\alpha\left[1/^{\circ}C^2\right]$ The temperature coefficient of the quadratic term is (-0.035 ± 0.005) × 10^-6/°C².

$T\left[^{\circ}C\right]$ Current temperature $T\left[^{\circ}C\right]$

$T_0\left[^{\circ}C\right]$ $T_0\left[^{\circ}C\right]$ Reference temperature (25 ± 5°C)



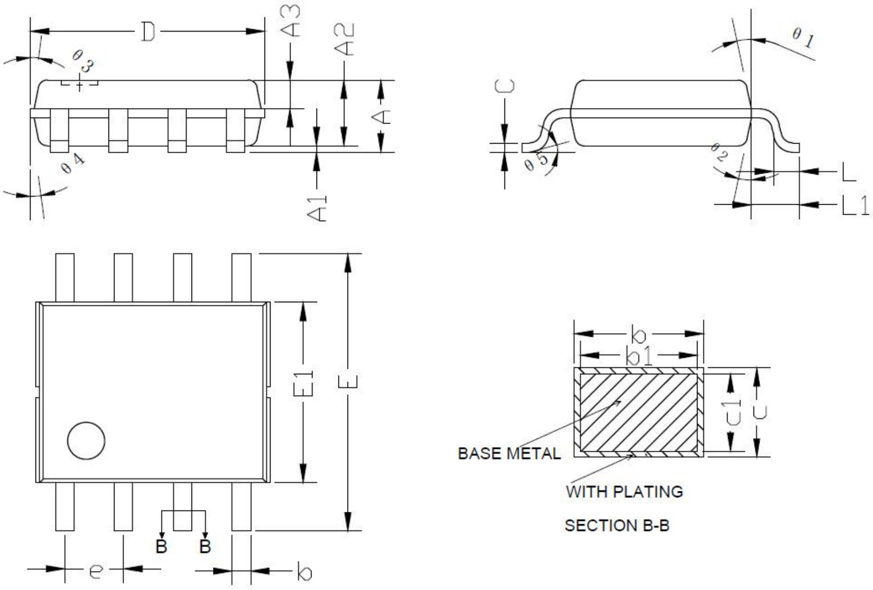
The clock chip's timing deviation (f/Δf) encompasses deviations caused by intrinsic frequency accuracy, frequency-temperature characteristics, and frequency-voltage characteristics. This deviation can be converted into daily timing error (s/d) using the following formula.

$$s/d = \Delta f / f \times 86400s$$

For example, a timing deviation of 11.574×10^-6 corresponds to a daily timing error of 1 second per day.

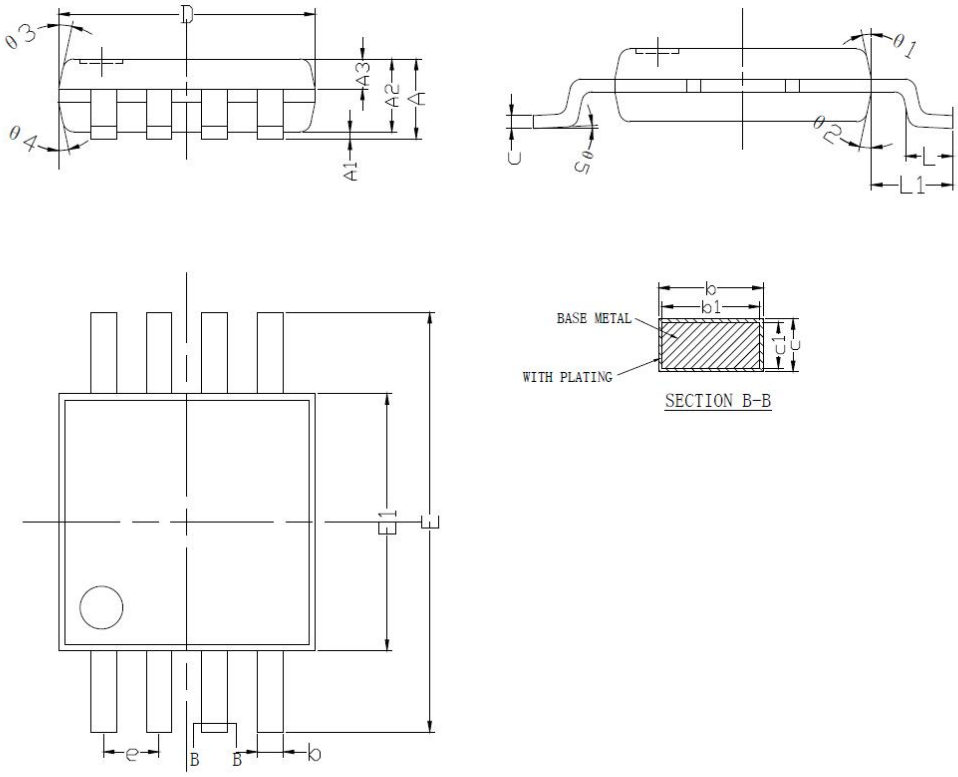
Package size

SOP8: 8-pin plastic package, body width 3.9mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.65
A1	0.10	--	0.25
A2	1.40	1.42	1.50
A3	0.57	0.62	0.67
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.90	6.00	6.20
E1	3.85	3.90	4.00
e	1.27(BSC)		
L	0.50	0.60	0.70
L1	1.05(BSC)		
θ1	9°	~	15°
θ2	9°	~	15°
θ3	8°	~	14°
θ4	8°	~	14°
θ5	0°	~	6°

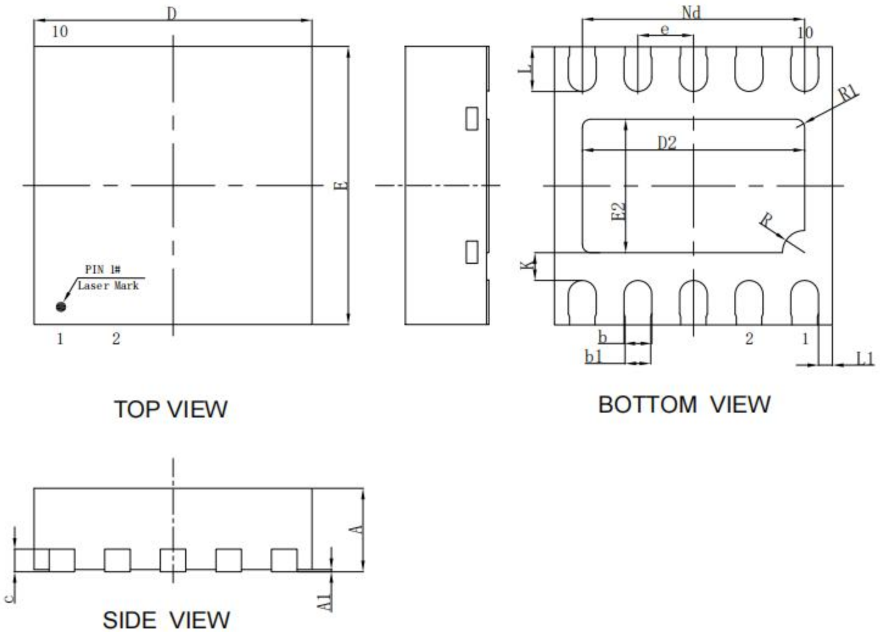
TSSOP8: 8-pin plastic package, body width 3mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.92	0.93	0.94
A1	0.03	0.08	0.13
A2	0.80	0.85	0.90
A3	0.299	0.349	0.399
b	0.23	--	0.37
b1	0.22	0.28	0.34
c	0.152	--	0.192
c1	0.142	0.152	0.162
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65(BSC)		
L	0.45	0.55	0.65
L1	0.95(BSC)		
θ1	10°	~	14°
θ2	10°	~	14°
θ3	10°	~	14°
θ4	10°	~	14°
θ5	1°	~	5°

DFN10

Body: Length*Width*Thickness 2.5mm*2.5mm*0.75mm-10L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 20	0. 25	0. 30
b1	0. 23REF		
c	0. 203REF		
D	2. 40	2. 50	2. 60
D2	1. 90	2. 00	2. 10
e	0. 50BSC		
Nd	2. 00BSC		
E	2. 40	2. 50	2. 60
E2	1. 10	1. 20	1. 30
L	0. 35	0.40	0. 45
L1	0. 125REF		
R	0. 20REF		
R1	0. 075REF		
K	0. 25REF		

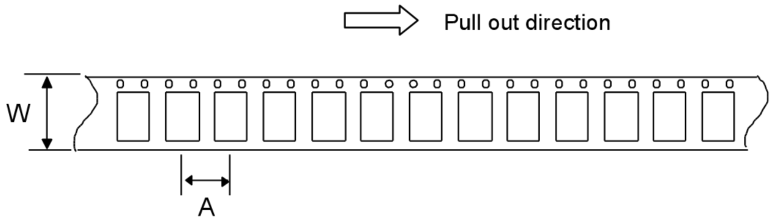
packing specifications

SOP8 & TSSOP8

Emboss Taping (TL)

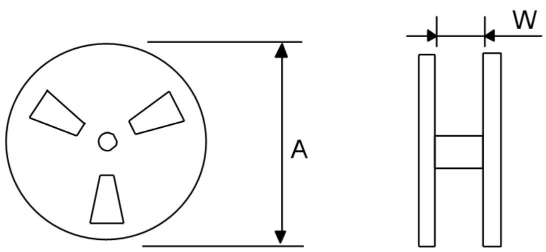
Symbol	SOP8 & TSSOP8
A	8
W	12

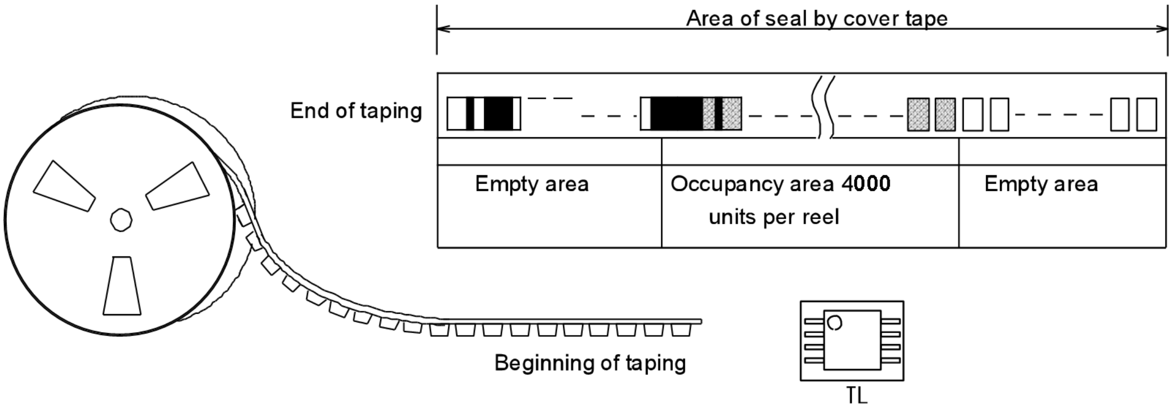
Unit : mm

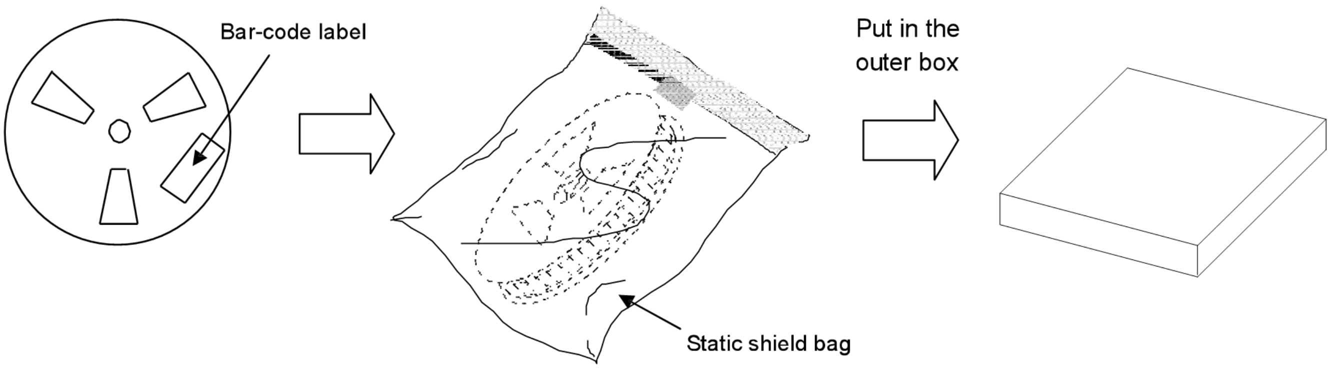


Symbol	SOP8 & TSSOP8
A	330
W	12

Unit : mm





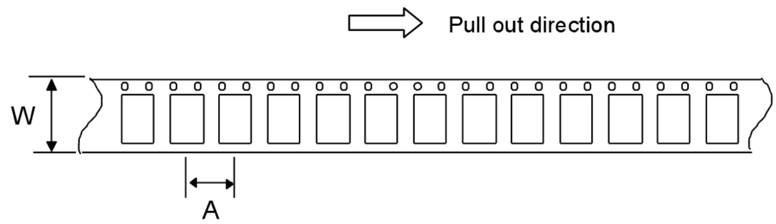


DFN10

Emboss Taping (TE2)

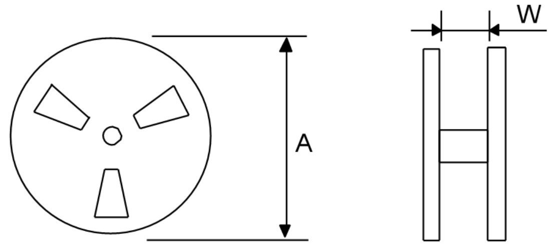
Symbol	DFN10
A	8
W	12

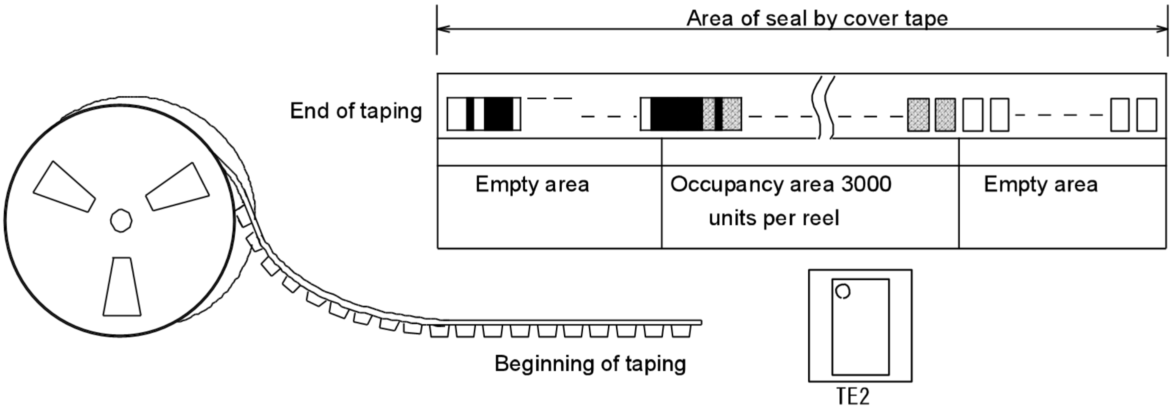
Unit : mm

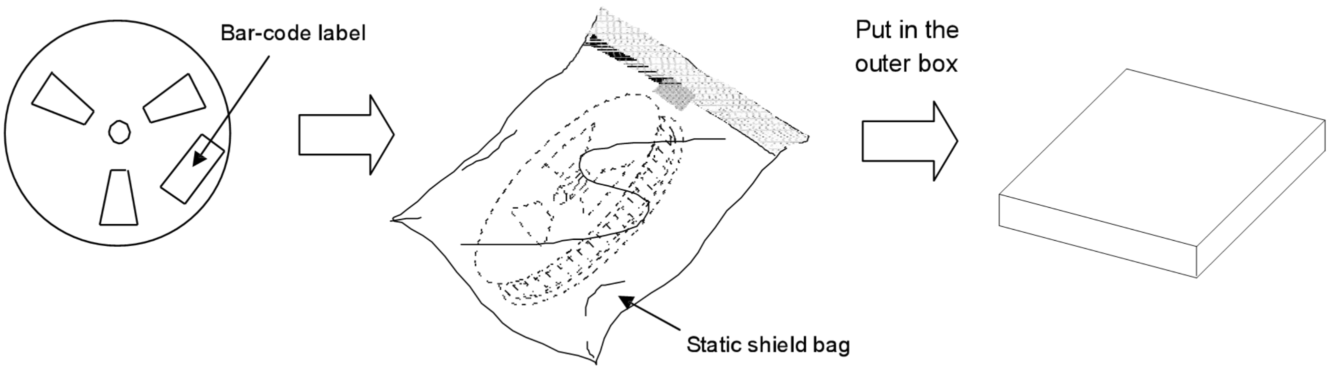


Symbol	DFN10
A	178
W	12

Unit : mm







Order Information

product name	material number	encapsulation form	Packaging format	Minimum order quantity
JXR2060	OSC0620600001000	SOP8	13-inch reel	4000
JXR2060-MS	OSC062060TS02000	TSSOP8	13-inch reel	4000
JXR2060-DS	OSC062060DS03000	DFN2525-10	7-inch reel	3000

Product Label Description