

JXR281T(LP) User Manual

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1 General Description

The JXR281T(LP) is an extremely accurate, IIC real-time clock (RTC) chip with built-in 32.768kHz digital temperature compensated crystal oscillator (D-TCXO). The minimum time unit is millisecond, and the automatic leap year correction is available. The JXR281T(LP) can also provide a timed alarm interruption, fixed-cycle interruption, time update interrupt output and frequency output at 32.768kHz, 1024Hz, 32Hz and 1Hz.

The chip operating temperature range covers $-45^{\circ}\text{C} \sim 125^{\circ}\text{C}$ and provides ultra-high precision clock output over temperature range of $-45^{\circ}\text{C} \sim 105^{\circ}\text{C}$, and also can provide absolute accuracy of $\pm 1^{\circ}\text{C}$ of temperature output. With time stamp function, it can be configured to be triggered by an external event or an internal event. Up to 8 groups of time stamps can be stored to record the event types and events triggered.

2 Features

- Built in extremely accurate 32.768kHz D-TCXO
- ms-level timing accuracy
- Fast (400kHz) IIC Interface support
- Operating Temperature Range of $-45^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- High frequency stability:
 - 25°C : $< 1.0\text{ppm}$; (daily timing error is less than 0.086s)
 - $0^{\circ}\text{C} \sim 50^{\circ}\text{C}$: $< 3.0\text{ppm}$; (daily timing error is less than 0.259s)
 - $-45^{\circ}\text{C} \sim 85^{\circ}\text{C}$: $< 5.0\text{ppm}$; (daily timing error is less than 0.432s)
 - $85^{\circ}\text{C} \sim 105^{\circ}\text{C}$: $< 8.0\text{ppm}$; (daily timing error is less than 0.691s)
- Time alarm interrupt (The interval can be set to week, day, hour and minute)
- Fixed-cycle interrupt
- Time update interrupt
- Frequency output at 32.768kHz, 1024Hz, 32Hz and 1Hz with enable control
- Calendar range supports 2000-2099, with automatic leap year correction
- Temperature compensation circuit operating voltage range: 2.2V \sim 5.5V
- Clock circuit operating voltage range: 1.0V \sim 5.5V
- Built-in 64Byte user RAM(when time stamp function disabled)
- Low current consumption: $0.9\mu\text{A}@3\text{V}(\text{Typ})$

3 Block Diagram

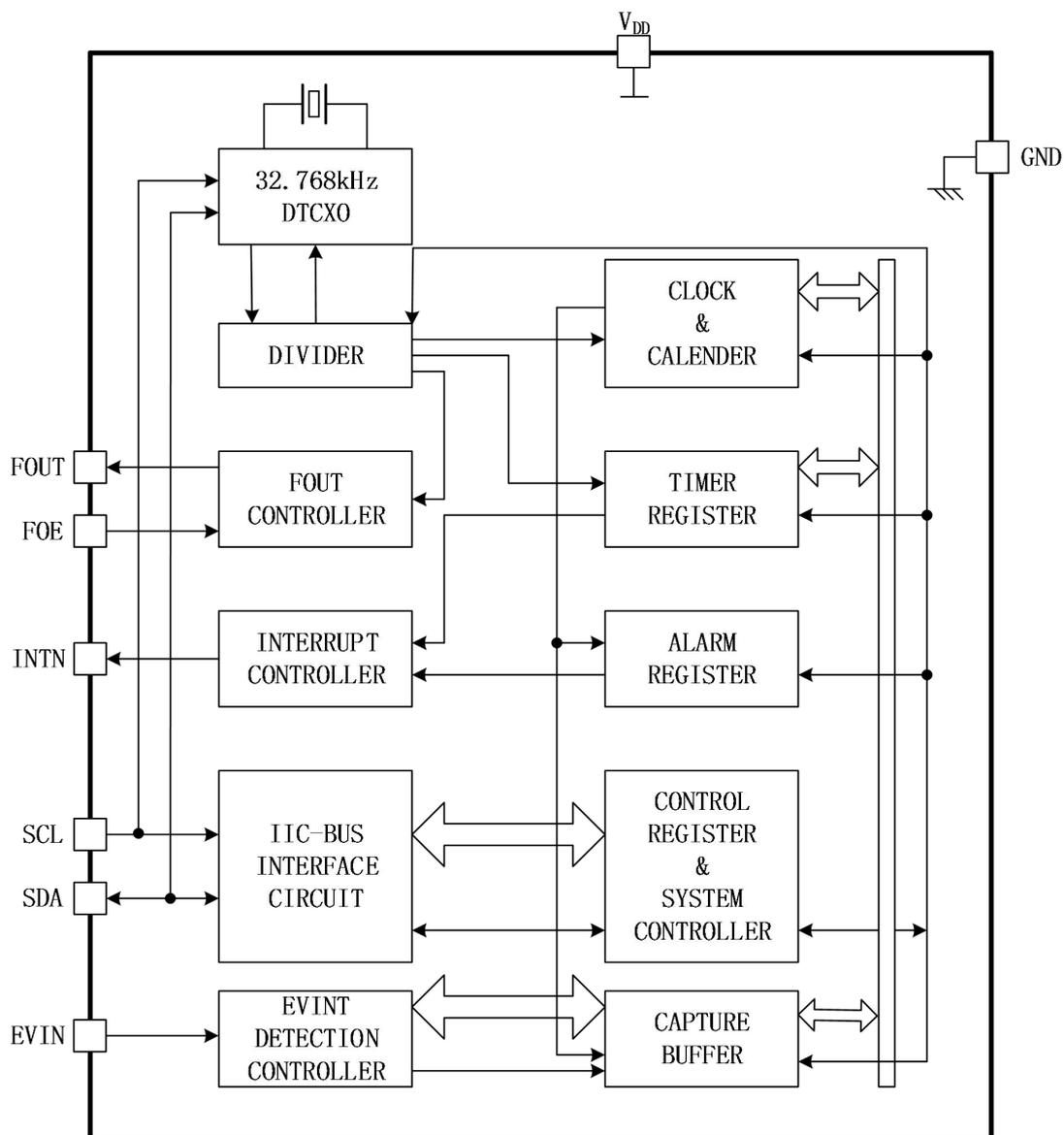


Figure 3-1 JXR281T(LP) Block Diagram

4 Pin Definitions

4.1 Pin Configuration

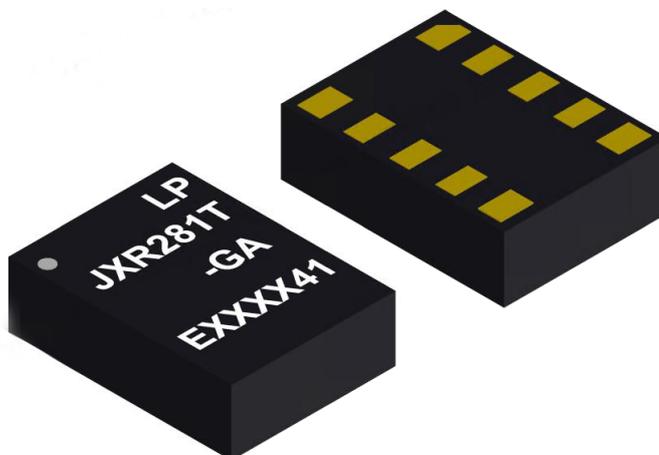


Figure 4- 1 JXR281T(LP) Pin Configuration

4.2 Pin Description

Table 4- 1 JXR281T(LP) Pin Description

Pin name	I/O	Function
1. FOE	INPUT	FOUT output enable, when FOE = '1', FOUT has frequency output
2. V _{DD}	POWER	Connect to VDD
3. EVIN	INPUT	External event-triggered time stamp interface that can configured for high pulse trigger mode or low pulse trigger mode.
4. FOUT	OUTPUT	32.768kHz frequency output port, controlled by FOE. When FOE = '1', this pin outputs a 32.768 kHz clock signal. When FOE = '0', the FOUT pin = Hi-Z (high impedance)
5. SCL	INPUT	Serial clock input pin for I2C-Bus communications.
6. NC	-----	No need to connect, stay suspended
7. SDA	INOUT	IIC bus communication data transmission side, N-ch open-drain output
8. NC	-----	No need to connect, stay suspended
9. GND	GROUND	Connect to GROUND
10. INTN	OUTPUT	Interrupt output port, N-ch open-drain output

5 Absolute Electrical Specifications

Table 5- 1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply Voltage* ¹	V _{DD}	Voltage between V _{DD} and GND	-0.5 to 6	V
Input Voltage* ^{1, *2}	V _{IN}	FOE, SCL, SDA, EVIN pins	-0.5 to V _{DD} + 0.5	V
Output Voltage* ^{1, *2}	V _{OUT}	FOUT, SDA, INTN pins	-0.5 to V _{DD} + 0.5	V
Storage Temperature Range	T _{STG}	Dispersed, unpackaged	-55 to 125	°C

*1: Each electrical specifications should not exceed the maximum rating range in the table above at any time, otherwise it will cause deterioration of the relevant parameters, decrease in reliability or even chip failure.

*2: V_{DD} here refers to the V_{DD} range under recommended operating conditions.

6 Recommended Operating Conditions

Table 6- 1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V _{DD}	Interface Voltage	1.5	3.0	5.5	V
Temperature Compensation operating Voltage	V _{TEM}	Temperature-Compensation Circuit Operating Voltage	2.2	3.0	5.5	V
Clock Operating Voltage	V _{CLK}	Oscillator Module Operating Voltage	1.0	3.0	5.5	V
Temperature Compensation Range	V _{COMP}	Temperature Compensation Operating Range	-45	25	105	°C
Operating Temperature	T _{OPR}	---	-45	25	125	°C

*Any operation outside of the recommended ranges in the table above may significantly affect the reliability of the chip.

7 Frequency Characteristics

Table 7- 1 Frequency Characteristics

Item	symbol	Condition	MIN	MAX	Unit
Frequency Stability	$\Delta f/f$	Ta = 25 °C, V _{DD} = 3.0V	-1.0	+1.0	×10 ⁻⁶
		Ta = 0 °C ~ 50 °C, V _{DD} = 3.0V	-3.0	+3.0	
		Ta = -45 °C ~ 85 °C, V _{DD} = 3.0V	-5.0	+5.0	
		Ta = 85 °C ~ 105 °C, V _{DD} = 3.0V	-8.0	+8.0	
		Ta = 105 °C ~ 125 °C, V _{DD} = 3.0V	-80.0	+10.0	
Voltage Coefficient	$\Delta f/f/V$	Ta = 25 °C, V _{DD} = 2.2V ~ 5.5V	-1.0	+1.0	×10 ⁻⁶ /V
Starting Time	T _{STA}	Ta = 25 °C, V _{DD} = 1.5V ~ 5.5V		1.0	s
		Ta = -40 °C ~ 85 °C, V _{DD} = 1.5V ~ 5.5V		2.0	
Aging	f _a	Ta = 25 °C, V _{DD} = 3.0V, first year	-1.0	+1.0	×10 ⁻⁶ /year

8 Electrical Characteristics

8.1 DC Electrical Characteristics

Table 8- 1 DC Electrical Characteristics

* Typical values are at GND = 0V, $V_{DD} = 1.5V \sim 5.5V$, $T_a = -40^{\circ}C \sim 85^{\circ}C$, unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Current Consumption	I_{DD1}	FOE = GND FOUT = '0'	$V_{DD} = 5V$		1.2	3.0	μA
	I_{DD2}		$V_{DD} = 3V$		0.9	2.0	
Current Consumption	I_{DD3}	FOE = V_{DD} FOUT = 32.768kHz CL = 0pF	$V_{DD} = 5V$		3.6		μA
	I_{DD4}		$V_{DD} = 3V$		2.9		
Current Consumption	I_{DD5}	FOE = V_{DD} FOUT = 32.768kHz CL = 30pF	$V_{DD} = 5V$		7.5		μA
	I_{DD6}		$V_{DD} = 3V$		6.2		
Current Consumption	I_{DD7}	During IIC communications, $V_{DD} = 5V$				5.0	μA
High Level Input Voltage	V_{IH}	FOE, SCL, SDA, EVIN pins	$V_{DD} = 2.2V \sim 5.5V$	$0.7 \cdot V_{DD}$		$V_{DD} + 0.3$	V
Low Level Input Voltage	V_{IL}	FOE, SCL, SDA, EVIN pins	$V_{DD} = 2.2V \sim 5.5V$	-0.3		$0.3 \cdot V_{DD}$	V
High Level Output Voltage	V_{OH}	FOUT pin	$I_{OH} = -1mA$	$V_{DD} - 0.3$		V_{DD}	V
Low Level Output Voltage	V_{OL}	FOUT, INTN pins	$I_{OL} = 1mA$	GND		$GND + 0.3$	V
		SDA pin	$V_{DD} \geq 2V$ $I_{OL} = 3mA$	GND		$GND + 0.3$	V
Input Leakage Current	I_{LK}	FOE, SCL, SDA, EVIN GND	$V_{IN} = V_{DD}$ or	-0.1		0.1	μA
Output Leakage current	I_{OZ}	INTN, FOUT, SDA, GND	$V_{IN} = V_{DD}$ or	-0.1		0.1	μA

8.2 AC Electrical Characteristics

Table 8- 2 AC Electrical Characteristics

*Typical values are at GND = 0V, V_{DD} = 1.5V ~ 5.5V, Ta = -40 °C ~ 85 °C, unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f _{SCL}	---			400	kHz
Starting Condition Setup Time	t _{SU:STA}	---	0.6			μs
Starting Condition Hold Time	t _{HD:STA}	---	0.6			μs
Data Transfer Setup Time	t _{SU:DAT}	---	100			ns
Data Transfer Hold Time	t _{HD:DAT}	---	0		700	ns
Termination Condition Setup Time	t _{SU:STO}	---	0.6			μs
Bus Idle Time	t _{BUF}	Between STOP and START Conditions	1.3			μs
Low Period of SCL	t _{LOW}	---	1			μs
High Period of SCL	t _{HIGH}	---	1			μs
SCL and SDA Rise Time	t _r	---			0.3	μs
SCL and SDA Fall Time	t _f	---			0.3	μs
Spike Time on Bus	t _{SP}	---			50	ns
FOUT Output Duty Cycle	Duty	Calculated with output up to 50% of V _{DD}	40	50	60	%

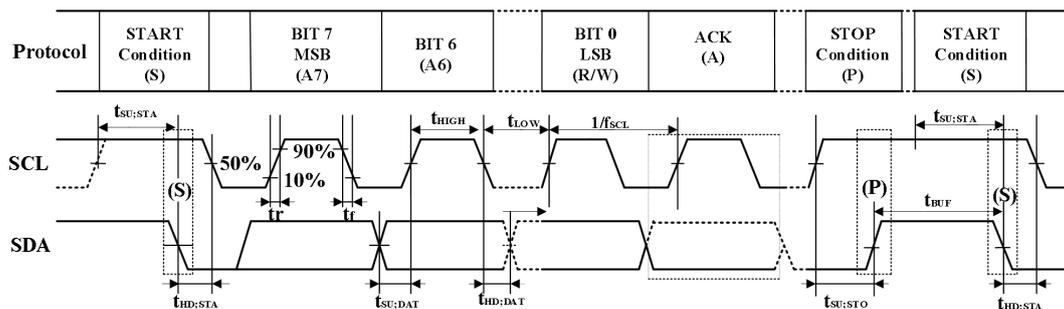


Figure 8- 1 IIC Timing

*The IIC data transfer is located between the STOP and START Conditions, the data transfer operation must be completed within 0.95s, after exceeding this event, the IIC bus will have an internal timer reset.

9 Registers

9.1 Registers Overview

Table 9- 1 Registers Summary Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70	MSEC[9:8]	○	○	○	○	○	○	512	256
71	MSEC[7:0]	128	64	32	16	8	4	2	1
00 or 10	SEC	○	40	20	10	8	4	2	1
01 or 11	MIN	○	40	20	10	8	4	2	1
02 or 12	HOUR	○	○	20	10	8	4	2	1
03 or 13	WEEK	○	6	5	4	3	2	1	0
04 or 14	DAY	○	○	20	10	8	4	2	1
05 or 15	MONTH	○	○	○	10	8	4	2	1
06 or 16	YEAR	80	40	20	10	8	4	2	1
07	RAM	●	●	●	●	●	●	●	●
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	●	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0B or 1B	TimerCounter0	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	○	○	○	○	2048	1024	512	256
0D or 1D	Extension	ETS	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	EVF	○	XST
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	EIE	EN_DET	RESET
17	Temp Int	SIGN	64	32	16	8	4	2	1
18	Temp Frac	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
1A	Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0
20 ~ 28	Time Stamp	Time Stamp 1/1024s → Year							
29	Stamp Status	EVTP1	EVTP0	○	○	○	○	SXST	○
2A	EVIN Setting	EHL	ET1	ET0	PDN	○	PU	OVW	○
2B	Command Trigger Ctrl	○	○	○	○	○	○	○	COMTG
2C	Command Trigger								
2D	TS Control0	○	○	○	○	○	EISEL	TSCLR	TSRAM
2E	TS Control1	○	○	PRCT1	PRCT0	○	○	○	EXST
2F	TS Control2	○	○	1'b1	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0
30 ~ 6F	TS RAM								

*Make sure to write valid values to the calendar and clock registers, otherwise the chip will not be able to perform correct timing operations.

*The register bits labeled '○' is a protected bit with a read value of '0'. Writing '1' to the protected bit is prohibited, otherwise it may cause chip function error. The register bits labeled '●' can be used as RAM to perform read and write operations.

*If the alarm interrupt function is not set (AIE = '0'), register 8~A can be used as RAM.

*If the interval timer interrupt function is not set (TE = TIE = '0'), register 0B or 1B and 0C or 1C can be used as RAM.

*UF, TF, AF and XST bits are only allowed to be written to '0'.

*When the chip is powered up, the CSEL0 bit is preset to '1', the FSEL1, FSEL0, CSEL1, UIE, TIE and AIE are preset to '0'.

* MSEC[9:8] and MSEC[7:0] are read-only registers.

9.2 Register Details

9.2.1 Clock and Calendar Registers (00 ~ 06 or 10 ~ 16)

- Data Structure

The contents except the WEEK register (register 3) are in the binary-coded decimal (BCD) format. For example, the value “0101 1001” of the Second register represents the current time is 59 second.

The timing system is fixed to 24-hour system.

- Year registers and leap years

The time range of the year register is 00 - 99. After 99, it overflows back to 00. When the value represented by the year register is divisible by 4, the year is recognized as a leap year. The valid time range of the calendar is 2000~2099.

- Week registers

The Day of the Week register has a total of 7 valid values, and each 1 valid bit represents one of the days from Monday to Sunday, so only one bit of this register is allowed to be '1'.

Table 9-2 Week Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Week
0	0	0	0	0	0	1	Sun.
0	0	0	0	0	1	0	Mon.
0	0	0	0	1	0	0	Tues.
0	0	0	1	0	0	0	Wed.
0	0	1	0	0	0	0	Thur.
0	1	0	0	0	0	0	Fri.
1	0	0	0	0	0	0	Sat.

9.2.2 Milliseconds Register (70 ~ 71)

These two registers are read-only registers and unable to write, and are used to provide ms timing for customers to get a more accurate clock than seconds. These two registers have a total of 10 valid bits (The high 2 bits are in register 70 and low 8 bits are in register 71), and the timing accuracy is (1/1024)s.

After the user configures the Seconds register, registers 70 and 71 are automatically cleared '0' and start from 0ms again.

9.2.3 Alarm Registers (08 ~ 0A)

Alarms can be set to X hours and X minutes on any day of the week or X hours and X minutes on day X of each month (weekly alarm mode and daily alarm mode), and the alarm code can be set by the WADA bit in register 0D or 1D.

Each alarm register has AE (Alarm Enable) bit (bit7). When the AE bit of a certain alarm register is '0', the set value of this register needs to be compared with the corresponding timing register, and an alarm interrupt is output when the value is the same; when the AE bit is '1', the corresponding alarm register value is ignored, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is the same as the corresponding timing register value.

When the WEEK Alarm mode is selected, the days of the week can be selected at the same time, so the WEEK Alarm function bit0~bit6 in register 0A or 1A can have several bits '1' at the same time.

The correspondences in the WEEK Alarm mode can be referred to Table9-3.

Table 9- 3 WEEK Alarm Mode Register A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0A	WEEK Alarm	Sat.	Fri.	Thur.	Wed.	Tues.	Mon.	Sun.

9.2.4 Fixed-Cycle Counter Control Register (0B or 1B and 0C or 1C)

These two registers are used to set the preset countdown value for the fixed-cycle interrupt. When the value in the above two registers changes from 001h to 000h, the fixed-cycle interrupt event occurs, TF is set to '1' and a low level is output on INTN (if TIE is '1'). After that, the 0B or 1B and 0C or 1C register are reset to the preset value, and the countdown process starts again.

9.2.5 Control Register and Flag Register(0D ~ 0F or 1D ~ 1F)

- ETS bit

EVIN trigger time stamp enable bit. When set to '1', the time stamp can be triggered by EVIN. When set to '0', the EVIN departure time stamp function is blocked.

- WADA bit

Alarm interrupt Mode Selection Bit. When set to '1', it is DAY Alarm Mode; when set to '0', it is WEEK Alarm Mode.

- USEL bit

Used to set the period of the time update interrupt; this bit default to '0' when the chip is powered up.

Table 9- 4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

When this bit is set to '1', the counter for fixed-cycle interruptions starts counting down, and when it is set to '0', it stops counting down.

- FSEL bit

It is used to set the output frequency of port FOUT. Refer to Table9-5 for the specific configurations. The bits are set to '00' after the chip is powered up by default.

Table 9- 5 FOUT Output Frequency Selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768kHz *Default
0	1	1024Hz
1	0	32Hz
1	1	1Hz

- TSEL bit

Used to set the count period for fixed-cycle interrupts.

Table 9- 6 Fixed-Cycle Interrupt Count Period Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF, EVF bit

Flag bits for alarm interrupt, fixed-cycle interrupt, time update interrupt and external event trigger time stamp; when the interrupt events above occur, the corresponding flag bit is set to '1'. The flag bit will be maintained as '1' until it is cleared to '0' manually, and it is prohibited to manually set the above fig bits to '1'.

- AIE, TIE, UIE, EIE bit

They are used to set the interrupt signal output on the INTN pin when an alarm interrupt, fixed-cycle interrupt, time update interrupt and time stamp event occurs . The all four bits is set to '0' by default when the chip is powered up.

The interrupt signal output on the INTN pin is the logical and of the alarm interrupt, fixed-cycle interrupt, time update interrupt and time stamp. The interrupt flag is used to determine the specific interrupt situation and to determine the interrupt signal output.

- XST bit

Oscillator stop flag. This bit is set to '1' after detecting that the crystal oscillator has stopped oscillating, causing the clock circuit to fail to time properly. This flag bit will remain '1' until it is manually cleared to '0'. Setting this flag bit to '1' manually is prohibited. This flag bit is set to '1' by default when chip is powered up, prompting the user that the current timing is not accurate and need to configure the time. After setting the time, you can set XST bit to '0' through IIC-bus, the flag bit will remain '0' until the oscillator stop event occurs.

- CSEL bit

Used to set the time interval for the temperature compensation circuit to start. This bit is set to '01' (2s) when the chip powered on.

Table 9- 7 Temperature Compensation Interval Selection

CSEL1	CSEL0	Operation interval
0	0	0.5s
0	1	2s *Default
1	0	10s
1	1	30s

- EN_DET bit

Oscillator Stop Detection function control bit. Setting this position to '1' turns on the stop oscillation detection function; setting this position to '0' turns off the stop vibration detection function, which saves about 50nA of current consumption. The default state of this control bit is '1' when chip is powered up.

- RESET bit

When RESET is set to '1', the Second and Millisecond register are reset, and the clock is stopped. Temperature compensation function is also disabled.

The RESET bit which is set to '1' will be re-cleared to '0' under the following three conditions: when an IIC stop condition is detected, a restart condition, or when the IIC bus is reset after 0.95s.

9.2.6 Temperature Registers (17, 18)

Table 9- 8 Temperature Related Registers Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17	Temp Int	SIGN	64	32	16	8	4	2	1
18	Temp Frac	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸

Registers 17 and 18 store the integer portion and the fractional portion of the current temperature value, where the highest bit of the register 17 is a sign bit, storing the data in the form of a 16bit signed number.

Table 9-9 Temperature Calculation Method

SIGN	Temperature Calculation Method
0	$T = reg17[6] \times 64 + \lambda + reg17[0] \times 1 + reg18[7] \times 2^{-1} + \lambda + reg18[0] \times 2^{-8}$
1	$T = reg17[6] \times 64 + \lambda + reg17[0] \times 1 + reg18[7] \times 2^{-1} + \lambda + reg18[0] \times 2^{-8} - 128$

For example,

Register 17, 18 are 0x19 and 0x80 representing the current temperature of 25.5°C.

Register 17, 18 are 0xFB and 0xC0 representing the current temperature of -4.25°C.

9.2.7 Output Precision Adjustment Register (1A)

The 1A register enables the function of fine-tuning the output frequency for higher timing accuracy. Refer to the following Table9-10 for the specific adjustment range and step size.

Table 9- 10 Output Frequency Accuracy Adjustment Table

OFS3	OFS2	OFS1	OFS0	Offset Value (ppm)
0	0	0	0	0.00
0	0	0	1	-0.55
0	0	1	0	-1.10
0	0	1	1	-1.65
0	1	0	0	-2.20
0	1	0	1	-2.75
0	1	1	0	-3.30
0	1	1	1	-3.85
1	0	0	0	4.40
1	0	0	1	3.85
1	0	1	0	3.30
1	0	1	1	2.75
1	1	0	0	2.20
1	1	0	1	1.65
1	1	1	0	1.10
1	1	1	1	0.55

9.2.8 time stamp Related Registers (20 ~ 6F)

Registers 20-28 are used to store the current time stamp, accurate to the ms level; registers 29-2F are time stamp function control bits; registers 30-6F can store 8 groups of time stamps, and if the time stamp function is disabled, this group of register can be used as ram.

Table 9- 11 Time Stamp Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20 ~ 28	Time Stamp	Time Stamp 1/1024s → Year							
29	Stamp Status	EVTP1	EVTP0	○	○	○	○	SXST	○
2A	EVIN Setting	EHL	ET1	ET0	PDN	○	PU	OVW	○
2B	Command Trigger Ctrl	○	○	○	○	○	○	○	COMTG
2C	Command Trigger								
2D	TS Control0	○	○	○	○	○	EISEL	TSCLR	TSRAM
2E	TS Control1	○	○	PRCT1	PRCT0	○	○	○	EXST
2F	TS Control2	○	○	1' b1	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0
30 ~ 6F	TS RAM								

*time stamp features are detailed in [Chapter 10](#).

10 Time Stamp Function

JXR281T(LP) has a time stamp function that can be configured to be triggered by external events, internal time or IIC commands, and can continuously store 8 sets of time stamps.

10.1 Function Description

The following three ways can trigger the time stamp function of the JXR281T(LP) chip.

- External event triggering (via EVIN Pin)
- Internal event triggering (crystal oscillator deactivation)
- IIC instruction triggered (via IIC operation of 2C registers)

After a time stamp event is triggered, the current time stamp is stored in the register at address 20-28, which can be configured to store the time stamp information in order in the RAM at address 30-6F.

10.2 General Controls

The time stamp information is stored in the corresponding registers and RAM in the form of Table 10-1.

Table 10- 1 Time Stamp Information Storage Format

Address	Function
20	1/1024s
21	30, 38, 40, 48, 50, 58, 60, 68
22	31, 39, 41, 49, 51, 59, 61, 69
23	32, 3A, 42, 4A, 52, 5A, 62, 6A
24	33, 3B, 43, 4B, 53, 5B, 63, 6B
25	WEEK
26	34, 3C, 44, 4C, 54, 5C, 64, 6C
27	35, 3D, 45, 4D, 55, 5D, 65, 6D
28	36, 3E, 46, 4E, 56, 5E, 66, 6E
29	37, 3F, 47, 4F, 57, 5F, 67, 6F
	Stamp Status

Users can configure with PRCT1 and PRCT0 not to repeat the trigger a number of times after a time stamp is triggered. Avoid the same event occurs, due to external noise interference caused by repeated generation of time stamps, occupy system resources.

Table 10- 2 Time Stamps Mask Setting

PRCT1	PRCT0	Description
0	0	No control over time stamp triggering
0	1	No new time stamps are triggered within 1sec
1	0	No new time stamps are triggered within 1min
1	1	No new time stamps are triggered within 5min

When a time stamp is triggered, not only the time information will be stored, but also the time stamp trigger type information will be synchronized and stored in EVTP1 and EVTP0, so that it is easy to find out the reason for triggering the corresponding time stamp.

Table 10- 3 Time Stamp Event Type Indication

EVTP1	EVTP0	Description
0	0	Non-triggered time stamp
0	1	External event (EVIN) trigger time stamp
1	0	IIC instruction trigger time stamp
1	1	Internal event (crystal oscillator deactivation) trigger time stamp

10.3 External Event (EVIN) Trigger Time Stamp

Table 10- 4 External Event Trigger Time Stamp Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	ETS	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	EVF	○	XST
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	EIE	EN_DET	RESET
2A	EVIN Setting	EHL	ET1	ET0	PDN	○	PU	OVW	○

- ETS bit

External event trigger time stamp function enable control, when EST is set to '1', the external event can trigger the time stamp through pin EVIN; when EST is set to '0', pin EVIN does not trigger the time stamp function back.

- EVF bit

External event trigger time stamp flag bit, when an external event triggers a time stamp via EVIN, the EVF bit is automatically set to '1', this bit will hold bit '1' until it is manually cleared to '0', it is prohibited to set this bit to '1' .

- EIE bit

Hardware interrupt enable control, when EIE is set to '1', after triggering the time stamp, the INTN pin outputs a low level; when EIE is set to '0', after triggering the time stamp, only a software response will be generated, and no interrupt information will be output through the INTN pin.

- EHL,PDN,PU bit

EHL controls external events by EVIN triggering time stamps, which need to be used in conjunction with PDN and PU. Specific controls can be found in the following table 10-5.

Table 10- 5 External Event Triggered Time Stamp Control Method

PDN	PU	EHL	Description
0	0	0	EVIN Pin requires external pull-up resistor, low pulse trigger time stamp
		1	EVIN Pin requires external pull-down resistor, high pulse trigger time stamp
0	1	0	EVIN Pin built-in pull-up resistor, low pulse trigger time stamp
		1	Invalid configuration
1	0	0	Invalid configuration
		1	EVIN Pin built-in pull-down resistor, high pulse trigger time stamp
1	1	0	EVIN Pin requires external pull-up resistor, low pulse trigger time stamp
		1	EVIN Pin requires external pull-down resistor, high pulse trigger time stamp

- ET1,ET0 bit

To prevent burrs on the EVIN pin from accidentally triggering the time stamp, a filter function can be configured to filter out unwanted interference. EVIN pulses below the set filter value will not trigger the time stamp.

Table 10- 6 EVIN Filter Settings

ET1	ET0	Description
0	0	No pulse width filtering
0	1	EVIN pulses with a pulse width less than 3.9ms will not trigger the time stamp
1	0	EVIN pulses with a pulse width less than 15.6ms will not trigger the time stamp
1	1	EVIN pulses with a pulse width less than 125ms will not trigger the time stamp

10.4 IIC Trigger Time Stamp

Table 10- 7 IIC Trigger Time Stamp Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2B	Command Trigger Ctrl	○	○	○	○	○	○	○	COMTG
2C	Command Trigger		2C	Command Trigger		2C	Command Trigger		2C

- COMTG bit

IIC event trigger time stamp enable control, when COMTG is set to '1', turn on the IIC event trigger time stamp function; when COMTG is set to '0', block the IIC event trigger time stamp function.

With the IIC event triggered time stamp function turned on, the time stamp is triggered by sending a read 2C register command over the IIC bus.

10.5 Internal Event (Crystal Oscillator Deactivation) Trigger Time Stamp

Table 10- 8 Internal Event Trigger Time Stamp Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29	Stamp Status	EVTP1	EVTP0	○	○	○	○	SXST	○
2E	TS Control1	○	○	PRCT1	PRCT0	○	○	○	EXST

- EXST bit

Internal event time stamp enable control, when EXST is set to '1', turn on the internal event trigger time stamp function; when EXST is set to '0', turn off the internal event trigger time stamp function.

- SXST bit

time stamp type indication bit, EVTP1 and EVTP0 are both '1', indicating that the current time stamp is triggered by an internal event, by confirming that the SCST bit is '1', it can be confirmed that a Oscillation stop has occurred.

10.6 Time Stamp RAM

Table 10- 9 Time Stamp RAM Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	EVIN Setting	EHL	ET1	ET0	PDN	○	PU	OVW	○
2D	TS Control0	○	○	○	○	○	EISEL	TSCLR	TSRAM
2F	TS Control2	○	○	1'b1	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0

- OVW bit

RAM address pointer cycle mode control, when OVW is configured as '1', it means that the time stamp information stored in RAM will cycle as FIFO (first-in-first-out); when OVW is configured as '0', the time stamp information stored in RAM will not cycle, and the new time stamps will be discarded when the memory is full.

Table 10- 10 Time Stamp RAM Cycle Control

OVW	Description
0	RAM address pointer does not cycle(000→001→...→111→stop)
1	RAM address pointer cycle(000→001→...→111→000→...)

- EISEL bit

Hardware interrupt output mode control bit, when EISEL is set to '1', it is the RAM FULL mode. After detecting the time stamp RAM is full, a hardware interrupt will be output; when EISEL is set to '0', for the normal interrupt mode, triggering the time stamp can generate hardware interrupt (note that the generation of hardware interrupt is also dependent on the state of the EIE).

- TSCLR bit

Used to initialize the RAM address pointer, when the TSCLR bit is set to '1', TSFUL is initialized to '1', and the TSEMP and TSAD bits are initialized to '1' .

- TSTRAM bit

RAM mode select bit, when TSTRAM is set to '1', the time stamp information is stored in register 20-29 while it will be synchronized to registers 30-6F; when TSTRAM is set to '0', the time stamp information is only stored in registers 20-29.

- TSFUL bit

RAM area full indicator bit, when the RAM area information storage is full, TSTRAM is set to '1' .

- TSEMP bit

RAM area empty indicator bit, when no time stamp information is stored in the RAM area, TSEMP is set to '1' .

- TSAD2,TSAD1,TSAD0 bit

Table 10- 11 RAM Pointer Correspondence

TSAD2	TSAD1	TSAD0	Address
0	0	0	30 ~ 37
0	0	1	38 ~ 3F
0	1	0	40 ~ 47
0	1	1	48 ~ 4F
1	0	0	50 ~ 57
1	0	1	58 ~ 5F
1	1	0	60 ~ 67
1	1	1	68 ~ 6F, Default

11 Interrupt Function

11.1 Alarm Interruption

Alarm interruptions can be generated on set days of the weeks, days, hours and minutes.

11.1.1 Alarm Interrupt Timing

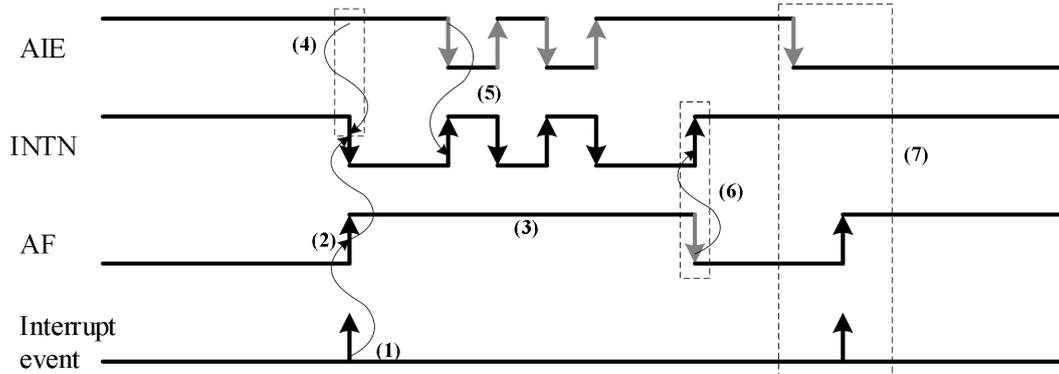


Figure 11-1 Alarm Interrupt Timing

- (1) Set the hour, minute, date or day of the week information corresponding to the alarm interruption and the WADA registers to generate an alarm interruption event when the set time matches the current time.
- (2) The AF flag bit is set to '1' when an alarm interrupt event is generated.
- (3) The AF register will remain at '1' until it is manually cleared to '0'.
- (4) When an alarm interrupt event occurs, if AIE='1', INTN outputs a low level; if AIE='0', INTN remains in a high resistance state.
- (5) If AIE is set to '0' during the INTN = '0' period, INTN will immediately return to the high resistance state; AIE can be used to control the output state of INTN before an alarm interrupt event occurs and the AF register is cleared to '0'.
- (6) Setting AF register to '0' clears the alarm interrupt output and INTN instantly changes from '0' to a high resistance state.
- (7) If AIE = '0' when the alarm interrupt time occurs, INTN stays high and does not output a low level.

11.1.2 Alarm Interrupt Related Registers

Table 11- 1 Alarm Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	●	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
0D or 1D	Extension	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	○	○	XTS
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET

- When configuring the Alarm Interrupt Register, it is recommended to first set AIE to '0' to prevent unnecessary hardware interrupts from being generated during operation.
- WADA is used to select the alarm mode, when set to '1', it is the DAY Alarm mode, when set to '0', it is the WEEK Alarm mode.
- The occurrence of an alarm interrupt event will set the AF flag position '1', which will remain at '1' until it is manually set to '0'.
- When an alarm interrupt event occurs, the AIE decides whether or not to generate an interrupt signal output (When AIE = '1', INRN = '0'; When AIE = '0', INTN = Hi-Z).
- AE bit of '0' indicates that the corresponding register needs to be compared with the clock or calendar register; if the AE bit is '1', the corresponding register is not compared, it is assumed that the register always matches the corresponding clock or calendar register. Refer to the following example:
 - (1) With register 0A is set to '80', only the minute alarm and HOUR Alarm registers need to be compared to the corresponding clock registers, ignoring the day of the week or date registers; therefore, an alarm interrupt event will be generated for each day as long as the hour and minute registers match.
 - (2) Setting the AE bits in each of the 08, 09, 0A register to '1' causes an alarm interrupt event to be generated once per minute.

11.2 Fixed-Cycle Interrupt

Fixed-cycle interrupts can generate interrupt alarm events at a fixed-cycle between 244.14 μ s and 4095min.

11.2.1 Fixed-Cycle Interrupt Timing

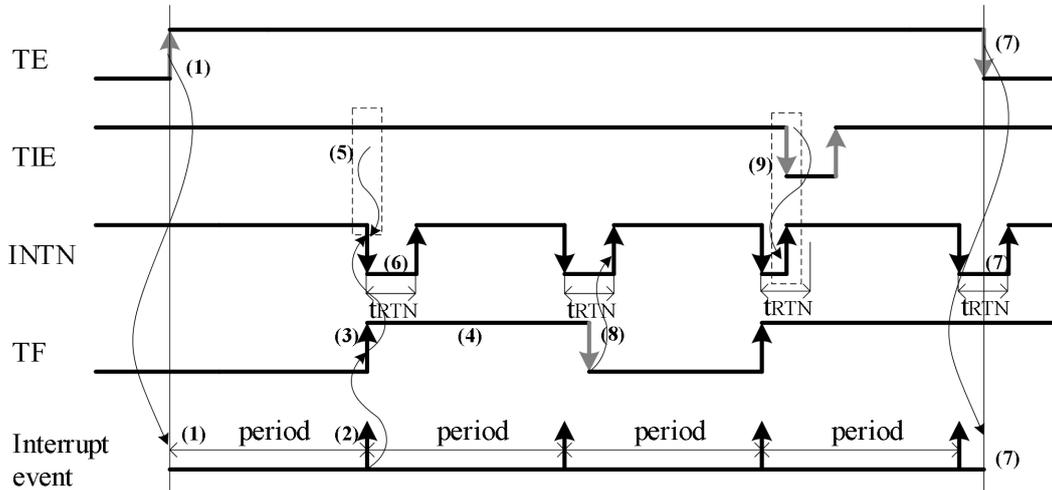


Figure 11-2 Fixed-Cycle Interrupt Timing

- (1) When '1' is written to the TE bit, the fixed-cycle counter starts counting down from the preset value.
- (2) When the fixed-cycle counter counts from 001h to 000h, an interrupt event is generated; the counter is reset to a preset value and continues to the next count.
- (3) When a fixed-cycle interrupt event occurs, the TF register is set to '1'.
- (4) The TF register will remain at '1' until it is manually cleared to '0'.
- (5) When a fixed-cycle interrupt event occurs, if TIE='1', INTN outputs a low level; if TIE='0', INTN remains in a high resistance state.
- (6) INTN output a low level for tRTN length of time, after which it will automatically restore a high resistance state until the next interrupt signal output.
- (7) When the TE bit is written to '0', the fixed-cycle counter stops counting and INTN outputs high resistance. (if TE is written to '0' during INTN='0', wait for tRTN time before INTN returns to the high resistance state.
- (8) If TF is cleared '0' during INTN=0, the high resistance state is restored after INTN continues for tRTN time.
- (9) When TIE writes '0', INTN instantly returns to the high-resistance state. If TIE is written to '1' again during tRTN, INTN returns to low level until tRTN ends.

11.2.2 Fixed-Cycle Interrupt Related Registers

Table 11-2 Fixed-Cycle Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B or 1B	TimerCounter0	128	64	32	16	8	4	2	1
0C or 1C	TimerCounter1	●	●	●	●	2048	1024	512	256
0D or 1D	Extension	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	○		XST
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET

- When configuring the fixed-cycle interrupt register, it is recommended that TE and TIE should be set to '0' first to prevent unnecessary hardware interrupts from being generated during operation.
- TSEL1 and TSEL0 are used to set the countdown period for fixed-cycle interrupts, and the automatic reset time of the interrupt signal on the INTN pin is related to the countdown period.

Table 11-3 Counting Period and Automatic Reset Time for Fixed-Cycle Interrupts

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122ms
0	1	64Hz	7.8125ms
1	0	1Hz	7.8125ms
1	1	1/60Hz	7.8125ms

- Registers 0B or 1B and 0C or 1C set the default value of the counter(001h ~ FFFh). The counter generates a fixed-cycle interrupt event when it counts down to 000h with the counting period set by TSEL.
- TE is the enable control bit of fixed-cycle counter, when TE='1', the counter starts counting down; when TE='0', the counter stops counting and terminates the fixed-cycle interrupt function.
- The occurrence of a fixed-cycle interrupt event will set the TF flag position '1', which will remain '1' until it is manually cleared '0'.
- When a fixed-cycle interrupt event occurs, TIE decides whether to generate an interrupt signal output or not.(When TIE = '1', INRN = '0'; When TIE = '1', INTN = Hi-Z)

Table 11-4 Example of a Fixed-Cycle Interrupt Cycle

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
.....
2048	500ms	32s	2048s	2048min
.....
4095	0.9998s	63.984s	4095s	4095min

11.3 Time Update Interruption

According to the set value, the time update interrupt generates an interrupt alarm event with a second update or a minute update.

11.3.1 Time Update Interruption Timing

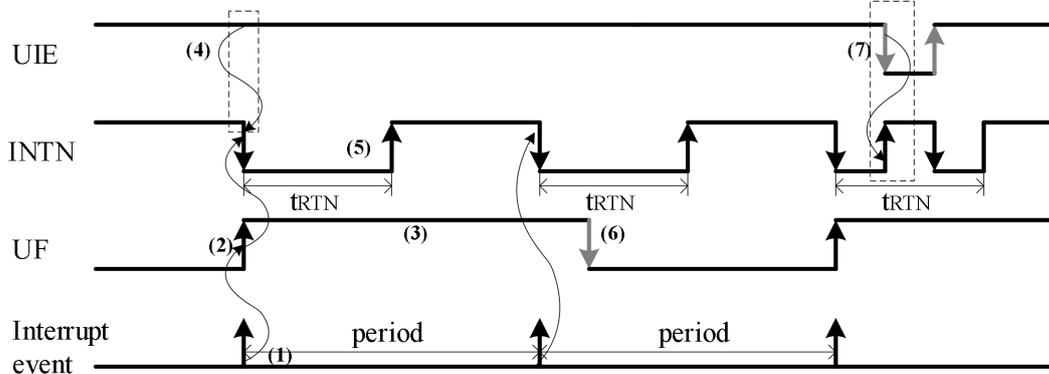


Figure 11-3 Time Update Interrupt Timing

- (1) USEL register determines whether the chip is in a second or minute update state. When the corresponding Second or Minute register updates, time update interrupt is generated.
- (2) UF register is set to '1' when time update interrupt occurs.
- (3) UF register will maintain '1' until it is manually cleared.
- (4) When time update interrupt occurs, if UIE = '1' INTN outputs 'L', if UIE = '0' INTN maintains 'Hi-Z'.
- (5) INTN outputs a low level voltage ('L') for the time length of t_{RTN} , after which it will automatically return to 'Hi-Z' until the next interrupt signal is output.
- (6) If UF is cleared (set to '0') during INTN = '0', INTN will recover to 'Hi-Z' after t_{RTN} .
- (7) IF UIE is set to '0' during INTN = '0', INTN recovers to 'Hi-Z' instantly and interrupt signal output stops. If UIE is set to '1' during t_{RTN} again, INTN recovers to 'L' until the end of t_{RTN} .

11.3.2 Time Update Interrupt Related Registers

Table 11-5 Time Update Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D or 1D	Extension	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E or 1E	Flag	○	○	UF	TF	AF	○	○	VDET
0F or 1F	Control	CSEL1	CSEL0	UIE	TIE	AIE	○	EN_DET	RESET

- It is recommended to set UIE to '0' before configuring time update interrupt register in case unwanted hardware interrupt is generated during the operation.
- USEL signal is used to set whether the interrupt mode is second update or minute update.

Table 11-6 Time Update Interrupt Mode Control

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of time update interrupt event will set UF to '1' and it maintains '1' until it is manually cleared.
- UIE determines whether or not to generate an interrupt signal output. (If UIE = '1', INTN = '0'. If UIE = '0', INTN = 'Hi-Z').

12 IIC-Bus Interface

12.1 Characteristics of IIC-Bus Interface

The IIC bus supports bi-directional communications, and its signal line SDA as well as the clock line SCL need to be connected to a high level voltage through a pull-up resistor. The port connected to the IIC bus must be open-drain in order to realize multi-device line connections.

12.2 Data Transfers

One bit of data can be transmitted per SCL clock cycle. When sending data, the data on the SDA line changes during SCL is 'L'. When receiving data, valid data can be obtained from the data line SDA during SCL is 'H'.

12.3 Starting and Stopping Conditions

In the idle state, both SCL and SDA are held high. During SCL is 'H', the falling edge of SDA is used as the start condition for IIC communication, and the rising edge of SDA is used as the stopping condition for IIC communication.

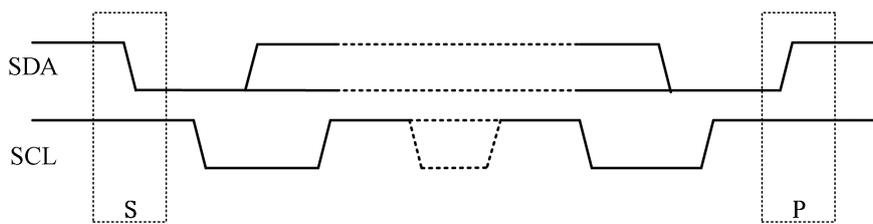


Figure 12- 1 IIC Starting and Stopping Conditions

12.4 Device Selection (Slave Address)

The IIC-Bus devices do not have any chip select or chip enable pins. The chip selection on the IIC-BUS is executed when the interface starts. The master device send the required slave address to all devices on the IIC-Bus. The slave device sends a acknowledge signal to setup communication with master device.

Slave address includes 7 bits of data ,4 bits (Group 1) + 3 bits(Group 2). The slave address of JXR281T(LP) is “0110010”. During the communication process, the slave address and R/W bit is sent as 8bit data.

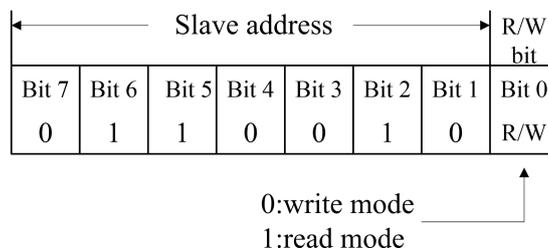


Figure 12-2 IIC Slave Address

12.5 System Configuration

The device that will control the data transfer becomes the master device and the devices that are controlled by the master device become the slave devices. The device that sends data is called the transmitter and the device that receives data is called the receiver.

In the JXR281T(LP) system, CPU or other controlling device become the master device and JXR281T(LP) itself becomes slave device. Both master and slave device can become transmitter or receiver.

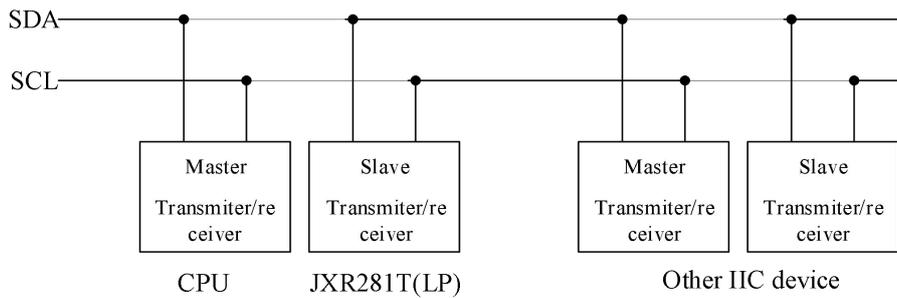


Figure 12- 3 IIC System Configuration

12.6 Acknowledge Signal

The IIC-bus has no limit on the number of bytes that can be transferred between the start and stop conditions. After each byte of data has been transferred, the transmitter releases the SDA bus and provides an SCL clock to receive an answer signal. If the receiver receives 8bit data successfully, it needs to set SDA to 0 after the end of the clock of transmitting the last 1bit data, and the transmitter will use this low level voltage as the answer signal for successful data transmission. After 1 clock cycle, the receiver releases the SDA bus and is ready to receive new data.

The IIC-bus terminates data transfer when the following conditions are met:

- (1)When the master device acts as the transmitter, it sends the termination condition after receiving the answer signal from the slave device.
- (2)When the master device acts as the receiver, it sends '1' as a acknowledge signal and then send a stop condition after receiving 8bit data successfully.

12.7 IIC-Bus Control

In the following sequence descriptions, it is assumed that the CPU is the master and the JXR281T(LP) is the slave.

12.7.1 Address Specification Write Operation

Since the JXR281T(LP) has address auto increment function, once the initial address has been specified, the JXR281T(LP) increments the receive address each time data is transferred automatically.

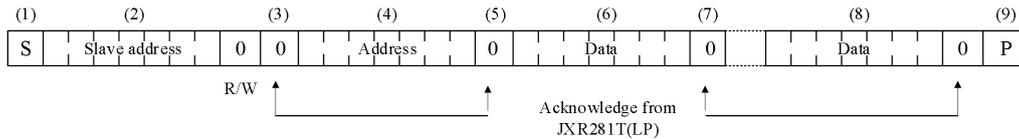


Figure 12- 4 Address Specification Write Operation

- (1) CPU transfers start condition [S].
- (2) CPU transfers the JXR281T(LP) 's slave address with the R/W bit set to write mode.
- (3) JXR281T(LP) generates acknowledge signal.
- (4) CPU transmits write address to JXR281T(LP).
- (5) JXR281T(LP) generates acknowledge signal.
- (6) CPU transfers write data to the address specified at (4) above.
- (7) JXR281T(LP) generates acknowledge signal.
- (8) Repeat (6) and (7) if necessary. Write addresses in JXR281T(LP) will increase automatically.
- (9) CPU transfers stop condition [P].

12.7.2 Address Specification Read Operation

After writing to the register, CPU can read the register by setting read mode.

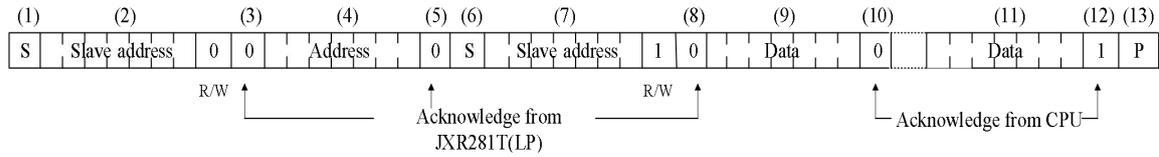


Figure 12-5 Address Specification Read Operation

- (1) CPU transfers start condition [S].
- (2) CPU transfers the JXR281T(LP)'s slave address with the R/W bit set to write mode.
- (3) JXR281T(LP) generates acknowledge signal.
- (4) CPU transmits read address to JXR281T(LP).
- (5) JXR281T(LP) generates acknowledge signal.
- (6) CPU transfers start condition again.
- (7) CPU transfers the JXR281T(LP)'s slave address with the R/W bit set to read mode.
- (8) JXR281T(LP) generates acknowledge signal, then CPU acts as receiver and JXR281T(LP) acts as a transmitter.
- (9) Data from address specified at (4) above is output by JXR281T(LP).
- (10) CPU generates acknowledge signal to JXR281T(LP).
- (11) Repeat (9) and (10) if necessary. Read addresses in JXR281T(LP) will increase automatically.
- (12) CPU generates acknowledge signal to JXR281T(LP).
- (13) CPU transfers stop condition [P].

12.7.3 Read Operation When Address is Not Specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address +1.

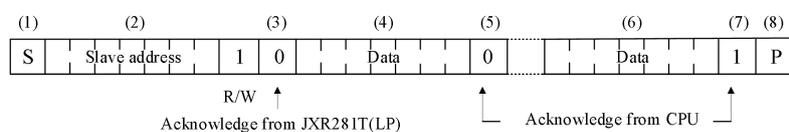


Figure 12-6 Read Operation When Address is Not Specified

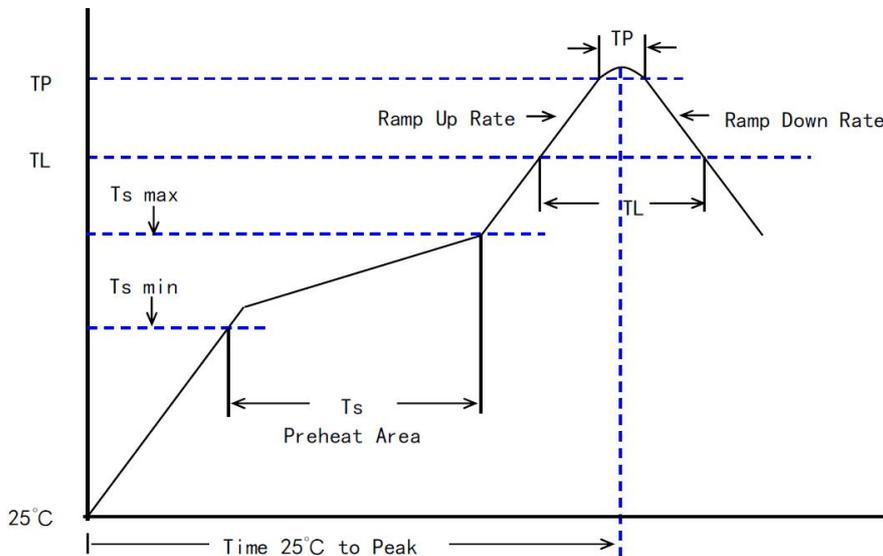
- (1) CPU transfers start condition [S].
- (2) CPU transfers the JXR281T(LP)'s slave address with the R/W bit set to read mode.
- (3) JXR281T(LP) generates acknowledge signal, then CPU acts as receiver and JXR281T(LP) acts as a transmitter.
- (4) JXR281T(LP) increase the read address automatically and transmit the data in the register.
- (5) CPU generates acknowledge signal.
- (6) Repeat (4) and (5) if necessary. Read addresses in JXR281T(LP) will increase automatically.
- (7) CPU generates acknowledge signal to JXR281T(LP).
- (8) CPU transfers stop condition [P].

Appendix

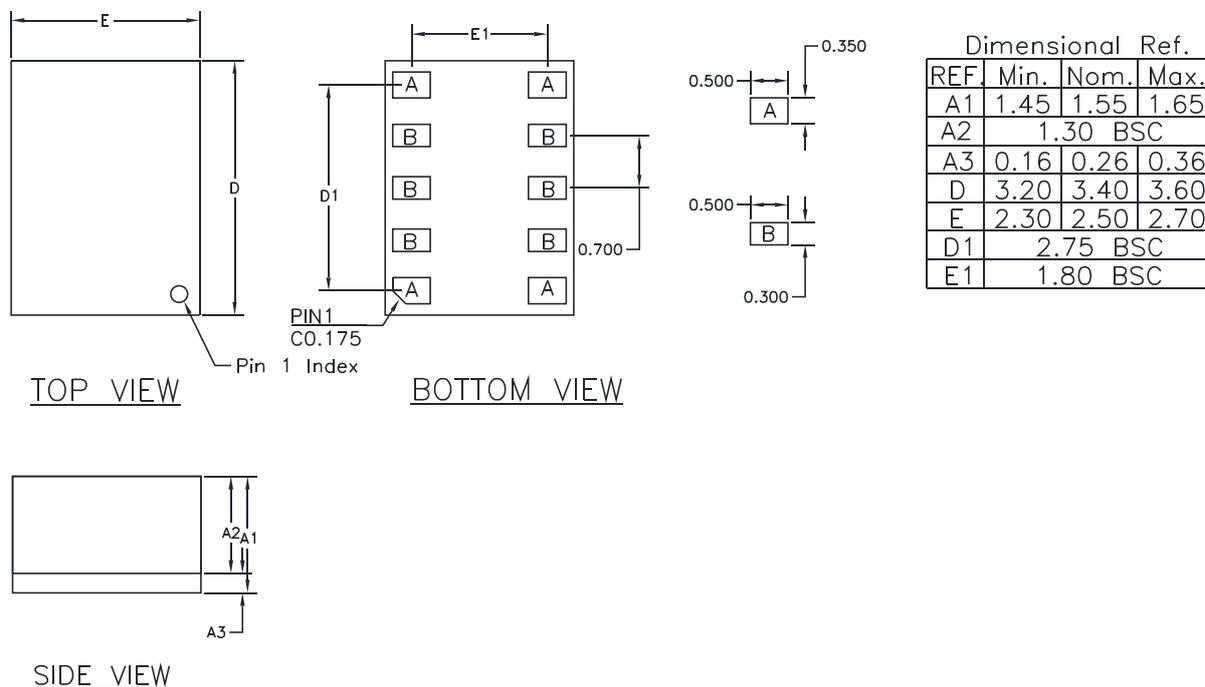
Instructions

1. Product electrostatic protection grade is HBM $\pm 2.0\text{kV}$, CDM $\pm 2.0\text{kV}$, which should be prevented from electrostatic breakdown during use.
2. In the process of product use, more than 8.25 volts of power supply spike may induce latch-up effect, leading to circuit damage. At least 0.1 μF decoupling capacitor should be added as close as possible to the power pin of the chip to ensure the chip's stability.
3. Since the chip is a low-power consumption IC, placing any noisy circuit components around the chip should be avoided.
4. Floating input pins may lead to increased current consumption. The chip's input pin should be connected to a fixed potential(VDD or GND) during use.
5. The chip has moisture sensitivity level of Level3. After unpacking and before welding, the workshop storage environment temperature should not exceed 30 °C , and the humidity should not exceed 60%RH, and the storage time should not exceed 168 hours.
6. Peak temperature needs to be strictly controlled not to exceed 260 °C during the reflow process, otherwise the built-in crystal oscillator may be damaged, resulting in excessive clock deviation or even stopping (recommended reflow parameters are as follows).

Profiles Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Min (Ts Min)	150°C
Temperature Max (Ts Max)	200°C
Time (Ts) from (Ts Min to Ts Max)	60 ~ 120 seconds
Ramp-up rate (TL to TP)	3°C/second Max
Liquidous Temperature (TL)	217°C
Time (TL) maintained above TL	60 seconds Max
Peak/Classification Temperature (TP)	245 \pm 5°C
Time within 5°C of actual Peak Temperature (TP)	10 seconds Max
Ramp-down rate (TP to TL)	6°C/second Max
Time 25°C to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max



Package Size



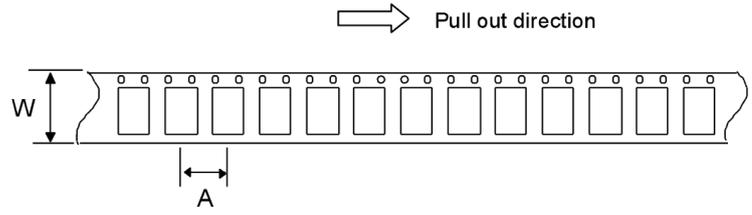
Unit: mm

Packaging Specification

Emboss Taping (TE2)

Symbol	LGA10
A	4
W	12

Unit : mm



Symbol	LGA10
A	330
W	12.4

Unit : mm

