

JXR201 User Manual

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1. Overview

JXR201 is a Low power consumption RTC module with IIC interface.

The minimum timing unit is second, can realize automatic leap year correction, and can provide alarm function, fixed-cycle Timer Interrupt function, time update interrupt function and 32.768KHz/1024Hz/1Hz clock output function.

2. Characteristics

- Built-in adjustable 32.768kHz crystal oscillator
- Supports IIC-Bus's high-speed mode (Up to 400 kHz)
- Multiple interrupt functions: timer alarm interrupt, fixed-cycle Timer Interrupt, time update interrupt
- 32.768KHz/1024Hz/1Hz clock output
- Support full calendar function from 2000 to 2099, support leap year automatic correction
- 32.768kHz/1024Hz/1Hz output
- Wide interface voltage range: 1.5V ~ 5.5V
- Wide time-keeping voltage range: 1.1V ~ 5.5V
- Built-in 128 bits RAM for users
- Low current power consumption: 0.5 μ A@3V(Typ)

3. Block Diagram

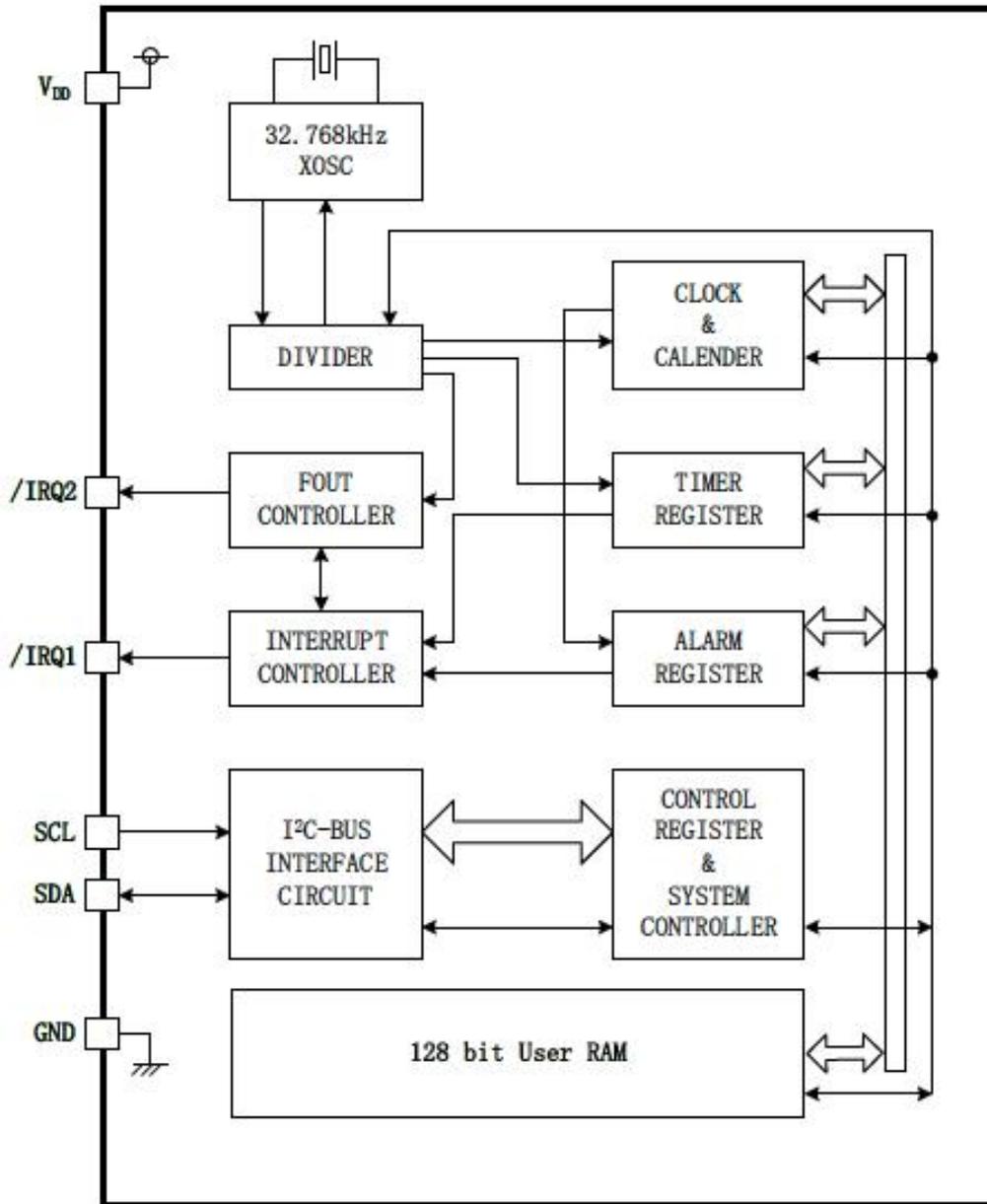


Figure 3- 1 JXR201 system block diagram

4. Terminal description

4.1 Package type

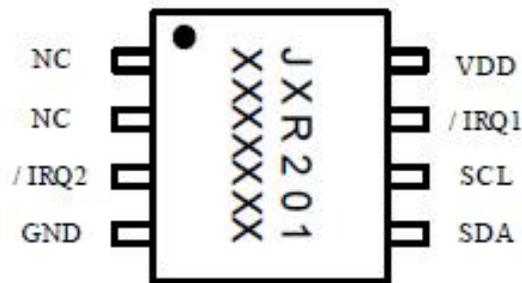


Figure 4- 1 JXR201 package form

4.2 Pin functions

Figure 4- 2 JXR201 Pin Description

Pin name	I/O	Function
1.2. NC	---	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.
3. /IRQ2	OUTPUT	Interrupt output pin, CMOS output(active low), which can be used for outputting timing interrupts and FOUT
4. GND	GROUND	Power grounding terminal
5. SCL	IN	This is the serial clock input pin for IIC Bus communications.
6. SDA	INOUT	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for IIC communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
7. /IRQ1	OUTPUT	Interrupt output pin, open-drain output(active low), which can be used for alarm interrupt, Fixed cycle interrupt and Time update interrupt and FOUT
8. VDD	POWER	This pin is connected to a positive power supply.

5. Absolute Maximum ratings

Table 5- 1 Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply voltage*1	V _{DD}	Voltage between V _{DD} and V _{SS}	-0.5 to 6	V
Input voltage*1, *2	V _{IN}	SCL, SDA pins	-0.5 to V _{DD} +0.5	V
Output voltage*1, *2	V _{OUT}	FOUT, SDA, INTN pins	-0.5 to V _{DD} +0.5	V
Storage temperature	T _{STG}	Store separately, unpacked	-55 to 125	°C

*1:Each electrical indicator shall not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of relevant parameters, reliability reduction and even chip failure.

*2:This V_{DD} refers to the range of V_{DD} under recommended operating conditions.

6. Recommended operating conditions

Table 6- 1 Recommend Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V _{DD}	Interface voltage	1.5	3.0	5.5	V
Clock supply voltage	V _{CLK}	operating voltage of Oscillator module	2.2	3.0	5.5	V
Maximum pull-up voltage	V _{pup}	SDA, /IRQ1 pins			5.5	V
Operating temperature range	T _{OPR}	---	-40	25	85	°C

* Any operation beyond the recommended range in the above table can greatly affect the reliability of the chip.

7. Frequency characteristics

Table 7- 1 Frequency Characteristics

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Frequency output	f _o		32.768 ^(Typ)			kHz
Frequency Stability	Δf/f	T _a =25°C, V _{DD} =3.0V	5±23			×10 ⁻⁶
Frequency/voltage characteristics	Δf/f/V	T _a =25°C, V _{DD} =1.1V~5.5V	-1.0		+1.0	×10 ⁻⁶ /V
Frequency-temperature characteristic	T _{op}	T _a =-20°C~70°C, V _{DD} =3.0V	-100		+10	×10 ⁻⁶
Oscillation start time	T _{STA}	T _a =25°C, V _{DD} =1.5V~5.5V			1.0	S
		T _a =-40°C~85°C, V _{DD} =1.5V~5.5V			3.0	
Aging	f _a	T _a =25 °C, V _{DD} =3.0V, first year	-5.0		+5.0	×10 ⁻⁶ /year

8. Electrical characteristics

8.1 DC Characteristics

Table 8- 1 DC Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I _{DD1}	F _{SCL} = 0Hz /IRQ1,2 = OFF	V _{DD} = 5.0 V		0.6	1.3	μA
	I _{DD2}		V _{DD} = 3.0 V		0.5	1.0	
	I _{DD3}	F _{SCL} = 0Hz /IRQ2 = OFF /IRQ1 = 32.768kHz	V _{DD} = 5.0 V		0.7	1.5	nA
	I _{DD4}		V _{DD} = 3.0 V		0.6	1.3	
	I _{DD5}	F _{SCL} = 0Hz /IRQ2 = 1024Hz CL = 15pF /IRQ1 = OFF	V _{DD} = 5.0 V		0.7	1.5	V
	I _{DD6}		V _{DD} = 3.0 V		0.6	1.3	V
High-level input voltage	V _{IH}	SCL, SDA, pins	V _{DD} = 1.5V ~ 5.5V	0.7*V _{DD}		V _{DD} +0.3	V
Low-level input voltage	V _{IL}	SCL, SDA pins	V _{DD} = 1.5V ~ 5.5V	- 0.3		0.3*V _{DD}	V
High-level output voltage	V _{OH}	/IRQ2 pin	I _{OH} = -1mA	V _{DD} - 0.3		V _{DD}	V
Low-level output voltage	V _{OL}	/IRQ1, /IRQ2 pins	I _{OL} = 1mA	GND		GND+0.3	V
		SDA pin	V _{DD} ≥ 2V I _{OL} = 3mA	GND		GND+0.3	V
Input leakage current	I _{LK}	Input Pins, V _{IN} =V _{DD} or GND		-0.1		0.1	μA
Output leakage current	I _{OZ}	Output Pins, V _{IN} =V _{DD} or GND		-0.1		0.1	μA

8.2 AC Characteristics

Table 8-2 AC Characteristics

Item	Symbol	Condition	Standard Mode			Fast Mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	---			100			400	KHz
Start condition setup time	$t_{SU;STA}$	---	4.7			0.6			μS
Start condition hold time	$t_{HD;STA}$	---	4.0			0.6			μS
Data setup time	$t_{SU;DAT}$	---	250			100			nS
Data hold time	$t_{HD;DAT}$	---	0			0			nS
Stop condition setup time	$t_{SU;STO}$	---	4.0			0.6			μS
Bus idle time	t_{BUF}	Between start condition and stop condition	4.7			1.3			μS
Time when SCL = "L"	t_{LOW}	---	4.0			1.0			μS
Time when SCL = "H"	t_{HIGH}	---	4.0			1.0			μS
Rise time for SCL and SDA	t_r	---			1.0			0.3	μS
Fall time for SCL and SDA	t_f	---			0.3			0.3	μS
Allowable spike time on bus	t_{SP}	---			50			50	nS
FOUT duty cycle	Duty	---	40	50	60	40	50	60	%

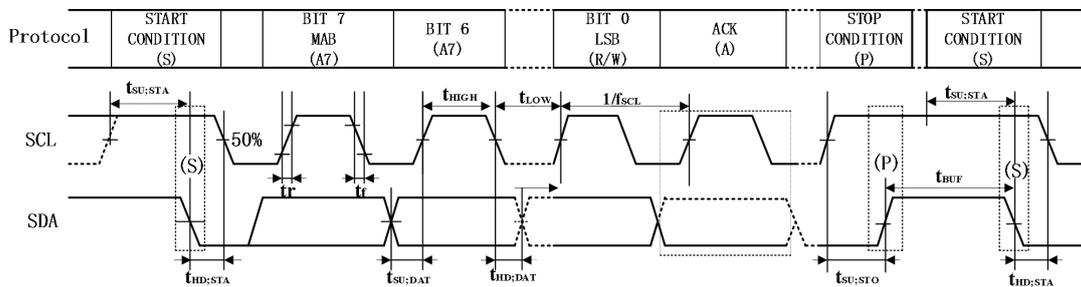


Figure 8-1 IIC timing legend

* The IIC data transfer is located between the start condition and the end condition, and the data transfer operation must be completed within 0.95S time, after which the IIC bus will be reset by the internal time.

9 Registers

9.1 Register summary table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10	SEC	○	40	20	10	8	4	2	1
11	MIN	○	40	20	10	8	4	2	1
12	HOUR	○	○	20	10	8	4	2	1
13	WEEK	○	6	5	4	3	2	1	0
14	DAY	○	○	20	10	8	4	2	1
15	MONTH	○	○	○	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	ANALOG	ADJ1	ADJ0	CL5	CL4	CL3	CL2	CL1	CL0
18	MIN Alarm	AE	40	20	10	8	4	2	1
19	HOUR Alarm	AE	•	20	10	8	4	2	1
1A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1B	Timer Counter 0	128	64	32	16	8	4	2	1
1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	○	STOP	UIE	TIE	AIE	TSTP	○	DETEN

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20 – 2F	RAM	User Register, 128 bits (16 * 8bits)							

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30	Digital Offset	DTE	L7	L6	L5	L4	L3	L2	L1
31	Soft Reset								
32	INT Ctrl Register	○	○	○	○	○	TMPIN	○	FOPIN

Table 9- 1 Register Table

* Make sure to write a legal value to the calendar clock register, otherwise the chip will not be able to perform the correct timing operation.

* Register bits marked with ○ are read-only bits and read values are "0";

* If the alarm interrupt is not set, reg 18h~1Ah can be used as RAM.

* If the Fix cycle interrupt is not set, reg 1Bh, 1Ch can be used as RAM.

* UF, TF, AF, VLF bits are only allowed to be written to "0".

* When the chip is powered on, the VLF bits are preset to "1", FSEL1, FSEL0, USEL, UIE, TIE, AIE bits are preset to "0".

9.2 Details of Registers

9.2.1 Time and date registers (Reg 10~16)

- **Data form**

With the exception of the week register (register 13), the data is in BCD code form. For example, the value "0101 1001" in the second register means that it is currently 59 seconds.

The timing mode is fixed to the 24-hour system.

- **Year register and leap year**

The year register ranges from 00 to 99, and then returns to 00 after 99; The year is a leap year when the value represented by the register is divisible by 4. The calendar is valid from 2000 to 2099.

- **Week Register**

The week register has a total of 7 significant bits (bit0~bit2) , showed on table 10-2.

table 9-2 Week register table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	week
0	0	0	0	0	0	1	日
0	0	0	0	0	1	0	一
0	0	0	0	1	0	0	二
0	0	0	1	0	0	0	三
0	0	1	0	0	0	0	四
0	1	0	0	0	0	0	五
1	0	0	0	0	0	0	六

9.2.2 Extended register(reg 17)

- **ADJ<1:0> bit**

Power consumption adjustment bits, by changing these bits, the current consumption of the RTC can be adjusted. Below is the specific adjustment reference.

table 9-3 Current consumption adjustment table

ADJ<1>	ADJ<0>	Current Consumption
0	0	550 nA
0	1	500 nA *Default
1	0	Forbidden
1	1	

- **CL<5:0> bit**

By adjusting the Cl bits, the output frequency accuracy can be tuned to achieve more precise timing accuracy. Below is the specific adjustment reference.

table 9- 4 Frequency adjustment table

CL<5>	CL<4>	CL<3>	CL<2>	CL<1>	CL<0>	Frequency Offset (ppm)
0	0	0	0	0	0	100
0	0	0	0	0	1	95.5
0	0	0	0	1	0	
.....						
0	1	1	1	1	0	4.6
0	1	1	1	1	1	2.3
1	0	0	0	0	0	0
1	0	0	0	0	1	-2.3
1	0	0	0	1	0	-4.6
.....						
1	1	1	1	0	1	-49.6
1	1	1	1	1	0	-50.8
1	1	1	1	1	1	-52.0

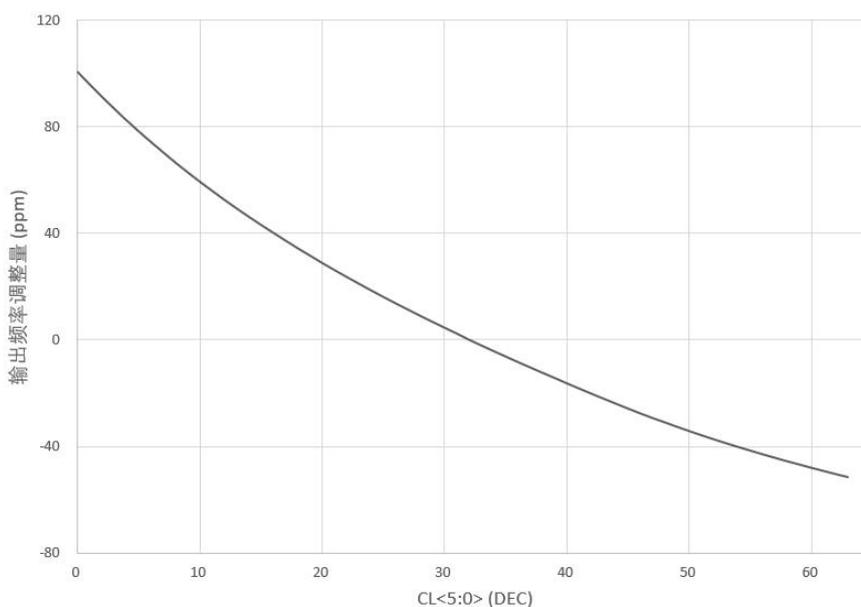


Figure 9- 1 FOUT adjustment step

9.2.3 Alarm register (Reg18~1A)

The alarm can be set to X hours X minutes on X days of the week or X hours X minutes on X days of the month (week alarm mode and day alarm mode), and the alarm mode can be set via the WADA bit of register 0D or 1D.

Each Alarm register has AE (Alarm Enable) bits (bit7). When the AE bit of an alarm register is "0", the set value of the register needs to be compared with the corresponding timer register. When the value is consistent, the output alarm is interrupted; If the AE bit is "1", the corresponding alarm register value is ignored, that is, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is consistent with the corresponding timing register value.

When the WEEK ALARM mode is selected, several days of the week can be selected at the same time, that is, the week alarm function bit0 to bit6 in register 0A can have several bits of "1" at the same time. Refer to Table 9-3

for the corresponding relationship in week alarm mode.

Table 9- 5 Week alarm mode register 0A table

Register	Function	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1A	Week alarm	Sat	Fri	Thu	Wed	Tue	Mon	Sun

9.2.4 Fixed cycle counter control register (register1B, 1C)

These two registers are used to set the preset backcount value of the fixed period interrupt. When the value in the above two registers changes from 001h to 000h, the fixed period interrupt event occurs, TF is set to "1" and INTN outputs a low level (if TIE is "1"); The 1B or 1C registers are then reset to the preset value and the countdown process is restarted.

9.2.5 Control register and Flag register (registers 1D~1F)

- FSEL bit

Set the output frequency of the FOUT port. For details, see Table 9-5. After the chip is powered on, the default value is 00.

Table 9- 6 FOUT output frequency selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768kHz * Default
0	1	1024Hz
1	0	1Hz
1	1	32.768kHz

- WADA bit

Alarm Interrupt mode selection bit, when set to "1", for daily alarm mode, when set to "0", for weekly alarm mode.

- USEL bit

The period used to set the time update interrupt; The bit is an indefinite value when the chip is powered on, and needs to be manually configured during use.

Table 9- 7 Time Update Interrupt mode selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

When the position is "1", the counter with fixed period interruption starts to count backwards, and when it is set to "0", it stops counting backwards.

- TSEL bit

The counting period used to set the fixed period interrupt.

Table 9-8 Fixed cycle interrupt count cycle selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF bit

They are alarm interrupt, fixed period interrupt, time update interrupt flag bits; When the above interrupt event occurs, the corresponding flag bit is set to "1". The flag bit will remain as "1" until it is cleared to "0" manually. Do not manually set the flag position to "1".

- AIE, TIE, UIE bit

They are used to set the interrupt signal output on the INTN pin when alarm interrupt, fixed period interrupt, time update interrupt event occurs; The power-on default value of the three bits is "0".

The interrupt signal output on the /IRQ pin is alarm interrupt, fixed period interrupt, time update interrupt logic or, through the interrupt flag bit to judge the specific interrupt situation and determine the interrupt signal output.

- VLF bit

Low voltage detection flag bit; This bit is set to "1" when the power supply voltage is detected to drop below 1.8V, causing the clock circuit to not work properly, or when the power-on reset signal is detected. This flag bit will remain as "1" until it is cleared to "0" manually. Manual setting of this flag position "1" is prohibited.

- STOP bit

When the bit is set to "1", it can stop the flipping of the clock below 1024Hz, causing the clock to stop. Meanwhile, it pauses the countdown of the configured fixed cycle interrupt until this bit is cleared to "0". The default state of this control bit is "0" when powered on.

- DETEN bit

Oscillation Stop Detection Function Control Bit: When this bit is set to 1, the oscillation stop detection function is enabled. When set to 0, the function is disabled, which can save 50nA of current consumption. The default state of this control bit upon power-up is 1.

- TSTP

In the fixed cycle interrupt, when this bit is set to 1, it can pause the current countdown. At this time, the current countdown value will be maintained until the bit is cleared to 0, and the countdown will continue from the paused value.

9.2.6 Digital Adjustment Register (Reg 30)

*This function can adjust the timing accuracy of the RTC registers, but it will not improve the accuracy of 32.768kHz.

By configuring this register, the RTC timing accuracy can be adjusted with the step of 3.05ppm, covering range from +192.26ppm~ - 195.5ppm

- DTE bit

Digital calibration function enable bit. When this bit is set to '1', the digital calibration function is enabled, starting a calibration every 10 seconds. The specific calibration value is controlled by lower 7 bits; When this bit is set to '0', the digital calibration function is disabled.

- L7~L1

Digital calibration values. According to the values, the length of the 4th to 5th second will be adjusted every 10 seconds, achieving time accuracy adjustment. Below is the specific adjustment..

Table 9- 9 Frequency adjust step

L7	L6	L5	L4	L3	L2	L1	L0	Offset Value (ppm)
0	1	1	1	1	1	1	0	+192.26
0	1	1	1	1	1	0	1	+189.21
0	1	1	1	1	0	1	0	+186.16
.....							
0	0	0	0	0	1	0	0	+6.10
0	0	0	0	0	0	1	1	+3.05
0	0	0	0	0	0	0	0	0.00
1	1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	1	0	-6.10
.....							
1	0	0	0	0	0	1	0	-189.21
1	0	0	0	0	0	0	1	-192.26
1	0	0	0	0	0	0	0	-195.31

Example

If the deviation value to be adjusted is positive: $L\langle 7:1 \rangle = Dec2Bin (OffsetValue / 3.05)$

If the deviation value to be adjusted is negative: $L\langle 7:1 \rangle = Dec2Bin [128 - (OffsetValue / 3.05)]$

The digital calibration function adjusts the internal clock frequency division, thus affecting the FOUT frequency output and fixed cycle interrupt.

- FOUT Function

1Hz frequency output: The output frequency fluctuates once every 10 seconds

1024Hz frequency output: The output frequency fluctuates once every 10 seconds

32.768kHz frequency output: The output frequency remains unaffected.

- Fixed cycle interrupt

When 64Hz, 1Hz, 1/60Hz, or 1/3600Hz is selected as counting period, the counting period will be affected, while 4096Hz is selected, it won't be affected.

9.2.7 Soft Reset Control register (reg 31)

By configuring this register to 0x55, the soft reset function of the clock chip can be achieved. The soft reset will perform a reset operation on all registers and digital logic of the clock chip.

Configuring the soft reset register should be a single IIC command. It is not recommended to perform write operations on 31h register together with other registers in the same command.

9.2.8 Interrupt Output Control register (reg 32)

- TMPIN bit & FOPIN bit

TMPIN is used to control which pin the fixed cycle interrupt outputs;

FOPIN is used to control which pin the FOUT outputs;

TMPIN	FOPIN	/IRQ2	/IRQ1
0	0	Fixed-cycle interrupt & FOUT	time update interrupt & alarm interrupt
0	1	Fixed-cycle interrupt	time update interrupt & alarm interrupt & FOUT
1	0	FOUT	time update interrupt & alarm interrupt & Fixed-cycle interrupt
1	1	Hi-z	time update interrupt & alarm interrupt & Fixed-cycle interrupt & FOUT

10 Interrupt function

10.1 Alarm interrupt

Alarm interrupts can generate an interrupt event for a set week, day, hour, or minute.

10.1.1 Alarm Interrupt Timing

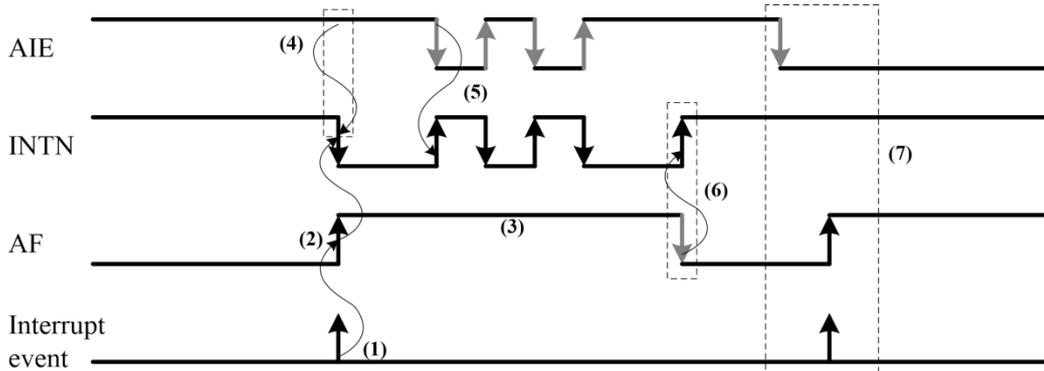


Figure 11- 1 Alarm interrupt sequence

(1) Set the hour, minute, date, or week corresponding to the alarm interruption. When the set time matches the current time (for details about the mapping, see Table 10-3), an interruption event is generated

(2) When the alarm interrupt event occurs, the AF flag bit is set to "1".

(3) The AF register will remain "1" until it is manually cleared to "0" via the IIC port.

(4) When the alarm interrupt event occurs, if AIE= "1", INTN outputs a low level; If AIE= "0", INTN remains Hi-Z

(5) If AIE is set to "0" during INTN= "0", INTN immediately returns to the Hi-Z state. AIE can be used to control the output state of INTN before the alarm interrupt event occurs and the AF register is cleared to "0"

(6) Clearing AF register "0" clears the alarm interrupt output, and INTN changes from "0" to Hi-Z status immediately

(7) If AIE= "0" when the alarm interrupt event occurs, INTN remains Hi-Z and does not output low, but the AF flag bit is set to "1".

10.1.2 Alarm interrupt related register

Table 11- 1 Alarm interrupt correlation register

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18	MIN Alarm	AE	40	20	10	8	4	2	1
19	HOUR Alarm	AE	•	20	10	8	4	2	1
1A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	○	STOP	UIE	TIE	AIE	TSTP	○	DETEN

- When configuring the alarm interrupt register, it is recommended to set AIE to "0" first to prevent unnecessary hardware interrupts during operation.
- WADA is used to select the alarm mode, when set to "1", daily alarm mode, when set to "0", weekly alarm mode.
- The occurrence of an alarm interruption event will set the AF flag position "1", which will remain "1" until it is set to "0" manually.
- When an alarm interrupt event occurs, AIE decides whether to generate an interrupt signal output (AIE= "1", then INTN= "0"; AIE= "0", then INTN=Hi-Z).
- An AE bit of "0" means that the corresponding register needs to be compared to a clock or calendar register; If the AE bit is "1", the corresponding register is not compared, that is, the register is always considered to match the corresponding clock or calendar register. Refer to the following example:
 - (1) When register 1A is set to "80", only the minute alarm and time alarm register need to be compared with the corresponding clock register, ignoring the day/date register; Therefore, as long as the hour register and the minute register match, an alarm interrupt event will be generated every day.
 - (2) 18, 19, 1A Setting the AE bits in all three registers to "1" will result in an alarm interrupt event every minute.

10.2 Fixed Cycle Interrupt Interrupt

Fixed period interrupts can generate interrupt events at a set period between 244.14 μ s and 255min.

10.2.1 Timed Interrupt Timing

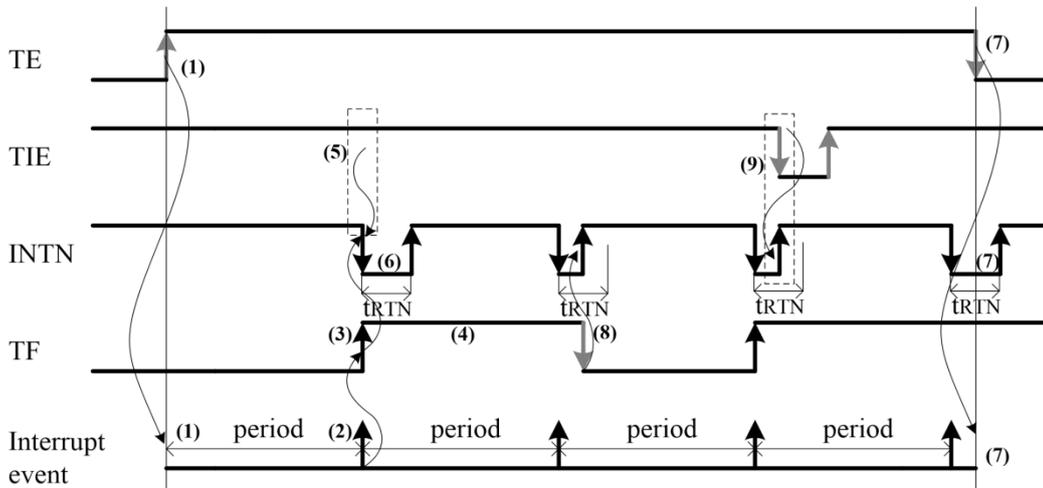


Figure 11- 2 Fixed-cycle Timer Interrupt Timing Chart

(1) When the TE bit is written to "1", the fixed period counter counts backwards from the preset value

(2) When the timer counter counts from 01h to 00h, an interrupt event is generated; Counter 0F resets to the preset value and continues the next backward count

(3) TF register is set to "1" when timed interrupt event occurs

(4) The TF register will remain in the "1" state until it is manually cleared to "0" via the IIC port

(5) When the timing interrupt event occurs, if TIE= "1", INTN outputs a low level; If TIE= "0", INTN remains Hi-Z

(6) INTN outputs the low level for t_{RTN} , and then automatically restores the Hi-Z state until the next interruption signal output, RTN as shown in Table 11-3.

(7) When TE bit writes "0", timing counter stops counting and INTN outputs Hi-Z (If TE write "0" occurs during INTN= "0", after t_{RTN} , INTN restores Hi-Z state)

(8) When TE bit writes "0", timing counter stops counting and INTN outputs Hi-Z (If TE write "0" occurs during INTN= "0", after t_{RTN} , INTN restores Hi-Z state)

(9) If TF is cleared "0" during INTN= "0", INTN immediately returns to the Hi-Z state (9)When TIE is written to "0", INTN immediately returns to Hi-Z

10.2.2 Fixed cycle interrupt related register

Table 11- 2 Fixed cycle interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	Timer Counter 0	128	64	32	16	8	4	2	1
1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	○	STOP	UIE	TIE	AIE	TSTP	○	DETEN

- When configuring the timed interrupt register, it is recommended to set TE and TIE to "0" first to prevent unnecessary hardware interrupts during operation.
- TSEL2 , TSEL1 and TSEL0 are used to set the inverted count period of the fixed period interrupt. The automatic reset time of the interrupt signal on the INTN pin is related to the inverted count period.

Fixed period interrupt count cycle and automatic reset time

TSEL1	TSEL1	TSEL0	Source clock	Auto reset time
0	0	0	4096Hz	0.122ms
0	0	1	64Hz	7.8125ms
0	1	0	1Hz	7.8125ms
0	1	1	1/60Hz	7.8125ms
1	0	0	1/3600Hz	7.8125ms

- Register 1B,1C sets the default value of the counter (001h~FFFh), which generates a fixed period interrupt event when the counter counts backwards to 000h in the counting period set by TSEL.
- TE is the enable control bit of the fixed period counter. When TE= "1", the counter starts to count backwards; When TE= "0", the counter stops counting and terminates the fixed period interrupt function.
- The occurrence of a fixed period interrupt event will mark TF position "1", which will remain "1" until it is manually set to "0".
- When a fixed period interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE= "1", then INTN= "0"; TIE= "0", then INTN=Hi-Z).

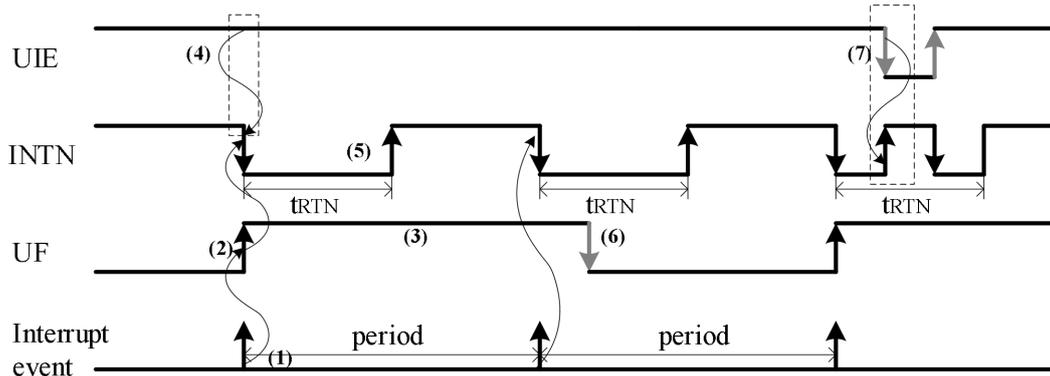
Table 10-4 Samples of fixed cycle interrupt cycle

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μs	15.625ms	1s	1min
.....
2048	500ms	32s	2048s	2048min
.....
4095	0.9998s	63.984s	4095s	4095min

10.3 Time Update Interrupt Function

Fixed period interrupts can generate interrupt alarm events at a fixed period between 244.14 μ S and 4095min.

10.3.1 Fixed cycle interrupt timing



(1) The USEL register determines whether the chip is in a second update interrupt or minute update interrupt state, and generates a time update interrupt event when the corresponding second register or minute register is updated.

(2) When the time update interrupt event occurs, the UF register is set to "1".

(3) The UF register will remain in the "1" state until it is cleared to "0" manually.

(4) INTN outputs a low level if UIE= "1" when the time update interrupt event occurs; If UIE= "0", INTN remains Hi-Z.

(5) INTN outputs a low level for tRTN, after which it automatically returns to Hi-Z status until the next interruption signal output.

(6) If UF is cleared to "0" during INTN= "0", INTN returns to Hi-Z after tRTN time.

(7) If UIE is set to "0" during INTN= "0", INTN immediately restores the Hi-Z state and the interrupt signal output ends. If UIE is written as "1" again during tRTN, INTN will remain in the Hi-Z state.

10.3.2 Time Update Interrupt related register

Time update interrupt registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	○	STOP	UIE	TIE	AIE	TSTP	○	DETEN

- When configuring the time update interrupt register, it is recommended to set the UIE to "0" first to prevent unnecessary hardware interrupts during operation.
- The USEL signal is used to set the interrupt mode to second update or minute update.

Time update interrupt mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event will leave the UF flag position "1", which will remain "1" until it is manually cleared to "0".
- When the time update interrupt event occurs, UIE decides whether to generate an interrupt signal output (UIE= "1", then INTN= "0"; UIE= "0", then INTN=Hi-Z).

11 IIC bus interface

11.1 IIC bus features

IIC is a two-way communication interface, its signal line SDA and clock line SCL need to be connected to VDD through pull-up resistance; The port connected to the IIC bus must be open-drain structure in order to realize the line and connection of multiple devices.

11.2 Data Transmission

1bit of data can be transferred per SCL clock cycle. When sending data, the data on the SDA line changes during the SCL low; When receiving data, stable and effective data can be obtained from the data line SDA during the high level of SCL.

11.3 Start condition and end condition

SCL and SDA remain high when idle. When SCL is high, the falling edge of SDA serves as the starting condition for IIC communication. During the high level of SCL, the rising edge of SDA is used as the termination condition of IIC communication.

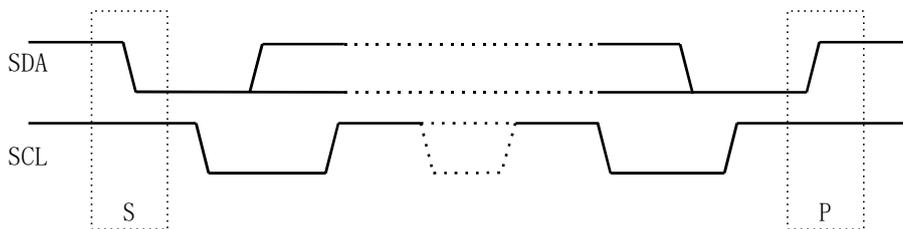


Figure 12- 1 IIC start condition and end condition

11.4 Device selection (from address)

The IIC bus device has no chip selection signal, the master device selects the corresponding slave device by sending a unique fixed device number (from the address), and the selected slave device sends a reply signal to establish communication with the master device.

The slave address includes 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2). The slave address of JXR201 is "0110010". During communication, the slave address and R/W select bits are sent as 8bit data.

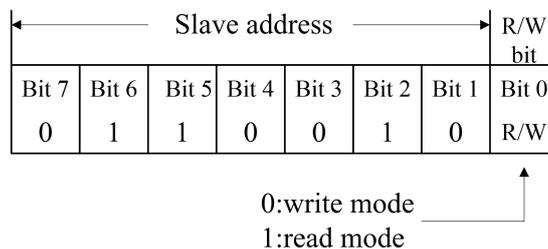


Figure 12- 2 IIC schematic from the address

11.5 System configuration

The device that controls data transmission is called the "master device" and the device controlled by the master device is called the "slave device"; The device that sends the data is called the "sending end" and the device that receives the data is called the "receiving end."

In a JXR201 system, the CPU or other control device is the primary device, and the

JXR201 chip itself is the secondary device; Both the master and slave devices can be used as sending or receiving ends.

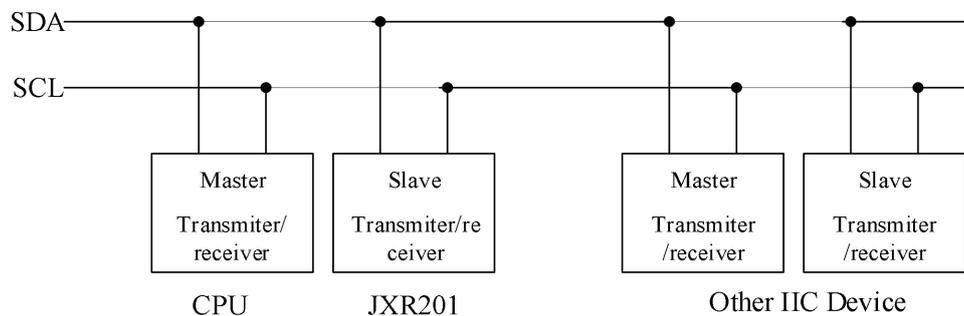


Figure 12- 3 IIC system configuration

11.6 Answer signal

The IIC bus has no limit on the number of bytes that can be transferred between the start and end conditions. After each byte of data is transferred, the sender releases the SDA bus and provides an SCL clock to receive the reply signal. If the receiver successfully receives 8 bits of data, the SDA must be set to "0" after the end of the clock for transmitting the last 1bit of data, and the sender will use this low level as the response signal of successful data transmission; After 1 clock cycle, the receiving end releases the SDA bus, ready to receive new data.

The IIC bus terminates the data transfer when the following conditions are met:

(1) When the master device acts as the sender, it sends the termination condition after receiving the reply signal from the slave device.

(2) When the master device acts as the receiver, after successfully receiving 8 bits of data, it sends a "1" as the reply signal and sends the termination condition immediately.

11.7 IIC bus control

This section describes the IIC bus communication timing for the CPU as the master device and the JXR201 as the slave device.

11.7.1 Specify address write operations

JXR201 has the address automatic increment function, after setting the operation address, only need to send data continuously, the address bit can be automatically incremented.

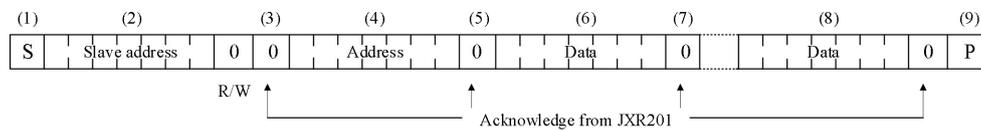


Figure 12- 4 Specify the address write operation

- (1) CPU send start condition [S].
- (2) The CPU sends JXR201 from the address and is set to write mode via R/W bit.
- (3) The JXR201 generates an answer signal.
- (4) The CPU sends the write register address to JXR201.
- (5) The JXR201 generates an answer signal.
- (6) The CPU sends data to the register corresponding to the address specified in (4).
- (7) The JXR201 generates an answer signal.
- (8) Repeat the process (6) (7) and the address of the write register in JXR201 will automatically increment.
- (9) CPU send termination condition [P].

11.7.2 Specify an address read operation

After writing to the register, the CPU can read the register data by setting the read mode.

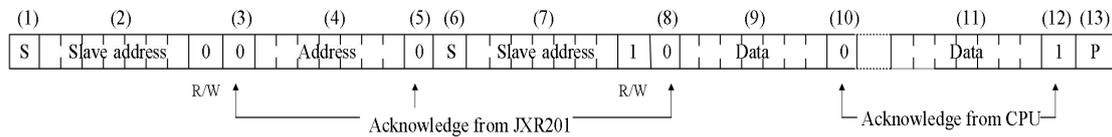


Figure 12- 5 specifies the address read operation

- (1) CPU send start condition [S].
- (2) The CPU sends JXR201 from the address and is set to write mode via R/W bit.
- (3) The JXR201 generates an answer signal.
- (4) The CPU sends the read register address to the JXR201.
- (5) The JXR201 generates an answer signal.
- (6) The CPU re-sends the start condition.
- (7) The CPU sends JXR201 from the address and is set to read mode via R/W bits.
- (8) JXR201 generates a response signal; After that, the CPU acts as the receiver and the JXR201 acts as the transmitter.
- (9) The JXR201 sends the data in the register corresponding to the address specified in (4)
- (10) The CPU sends a reply signal to the JXR201.
- (11) Repeat the process (9) (10) and the address of the read register in JXR201 will automatically increment.
- (12) The CPU does not send a reply signal to JXR201; The JXR201 switches to the IIC data receiver.
- (13) CPU send termination condition [P].

11.7.3 Address read operation not specified

The master device goes directly into read mode to read the contents of all registers from the device. The read operation address is the last IIC operation address +1.

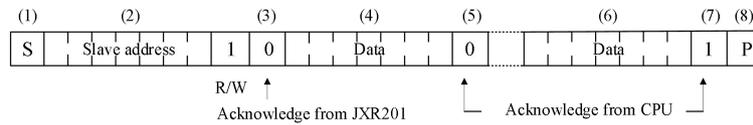


Figure 12- 6 does not specify the address read operation

(1) CPU send start condition [S].

(2) The CPU sends the JXR201 slave address and is set to read mode via R/W bit. The JXR201 generates an answer signal; After that, the CPU acts as the receiver and the JXR201 acts as the transmitter.

(3) The JXR201 automatically increments the register address and sends the register data.

(4) The CPU sends a reply signal to the JXR201.

(5) Repeat the process (4) (5) and the address of the read register in JXR201 will automatically increment.

(6) The CPU does not send a reply signal to the JXR201; The JXR201 switches to the IIC data receiver.

(7) CPU send termination condition [P]

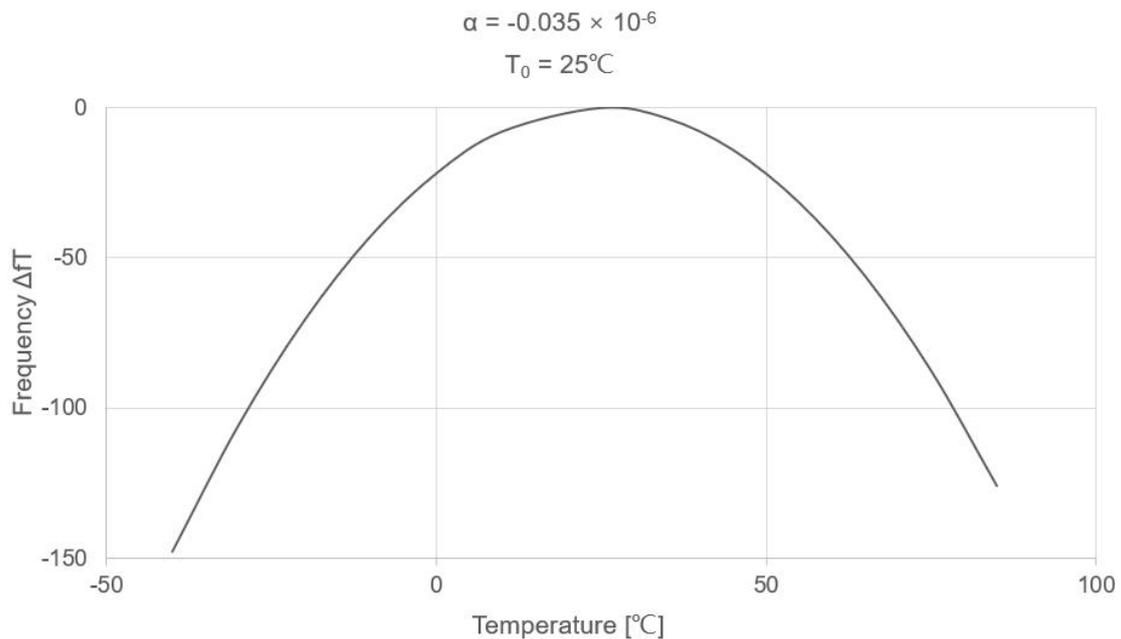
Appendix

Timing accuracy

The temperature characteristics of the clock chip's output frequency can be calculated using the following formula:

$$\Delta fT = \alpha (T - T_0)^2$$

ΔfT	: frequency deviation
$\alpha [1/^\circ\text{C}^2]$: Temperature coefficient $(-0.035 \pm 0.005) \times 10^{-6}/^\circ\text{C}^2$
$T [^\circ\text{C}]$: current temperature
$T_0 [^\circ\text{C}]$: reference temperature



The time deviation of the RTC includes deviation caused by intrinsic frequency accuracy, frequency-temperature characteristics, and frequency-voltage characteristics. The timing deviation can be converted into daily timing error(s/d) using the following formula.

$$s/d = \Delta f / f \times 86400s$$

For example, 11.57ppm=1s/d

Instructions

(1)The product's ESD level: HBM±2.0kV, CDM±2.0kV,so it is advised to take measures to prevent electrostatic breakdown.

(2) During product operation, power supply spikes exceeding 8.25V may induce latch-up effects, leading to circuit damage. A decoupling capacitor of at least 4.7uF should be added as close as possible to the power pin of the clock chip to ensure stable chip operation

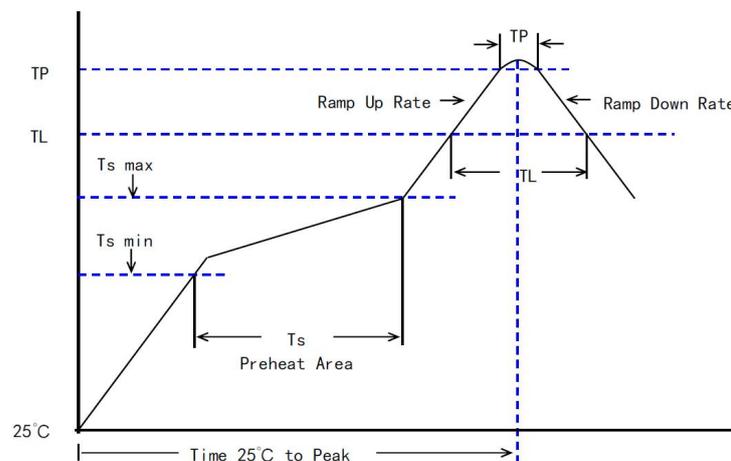
(3)Since the clock chip is a low-power integrated circuit product, any high-noise circuit components should be avoided from being placed around the clock chip.

(4) It is advised that the input pins be connected to a fixed potential.

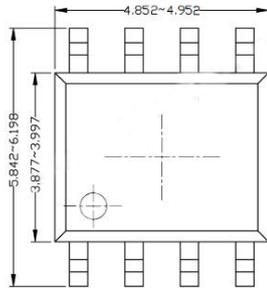
(5) The chip has a moisture sensitivity level of 3. Before unpacking and soldering onto the board, the storage environment should have a temperature and humidity not exceeding 30oC and 60%RH and the storage time should not exceed 168 hours

(6) During reflow soldering, the peak temperature must be strictly controlled within 260°C,and a maximum of 2 reflow soldering process are supported. For manual soldering, the temperature shall not exceed 350°C and the soldering time shall not exceed 5 secs. Otherwise, the built-in crystal oscillator may be damaged, leading to oscillator failure. Below is the recommended reflow curve

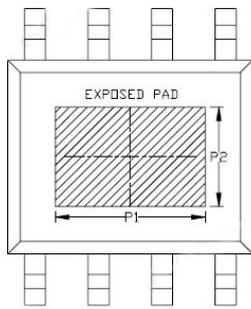
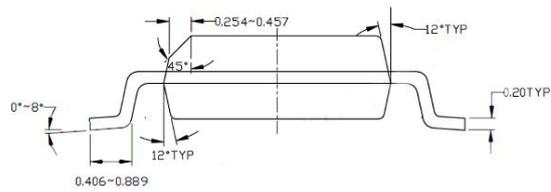
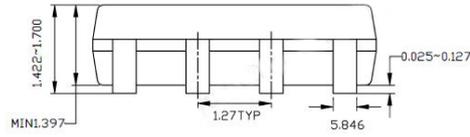
Profiles Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts Min) Temperature Max (Ts Max) Time (Ts) from (Ts Min to Ts Max)	150°C 200°C 60 ~ 120 seconds
Ramp-up rate (TL to TP)	3°C/second Max
Liquidous Temperature (TL) Time (TL) maintained above TL	217°C 35 seconds Max
Peak/Classification Temperature (TP)	245±5°C
Time within 5°C of actual Peak Temperature (TP)	5 seconds Max
Ramp-down rate (TP to TL)	6°C/second Max
Time 25°C to peak temperature	8 minutes Max
Suggest reflow times	3 Times Max



Package size



TOP VIEW



BOTTOM VIEW

Table for SDIC-EP8 of exposed die pad size.

Material Code.	Pad Size	Symbol	Min	Nom	Max
2004023855	3.302*2.413	P1	3.202	3.302	3.402
		P2	2.313	2.413	2.513

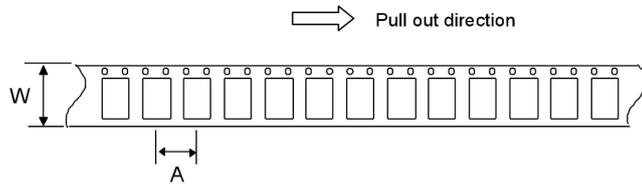
Unit:mm

Packing specification

Emboss Taping (TE2)

Symbol	SOIC-EP8
A	8
W	12

Unit : mm



Symbol	SOIC-EP8
A	330
W	12

Unit : mm

