JXR260-GA User Manual

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Content

1 Overview

JXR260-GA is a CMOS Real-Time Clock with IIC interface and calendar optimized for low power consumption. The minimum timing unit is second, can realize automatic leap year correction, and can provide alarm function, fixed-cycle Timer Interrupt function and 32.768KHz/1024Hz/32Hz/1Hz clock output function.

2 Characteristics

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz crystal
- Supports I2C-Bus' s high speed mode (400kHz)
- Alarm interrupt function for week, day, date, hour, and minute settings
- Fixed-cycle timer interrupt function
- 32.768kHz/1024Hz/32Hz/1Hz output
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 1.8V~5.5V
- Wide time-keeping voltage range: 1.0V~5.5V
- Low current consumption: 0.7μA@3V(Typ)

3 Block Diagram

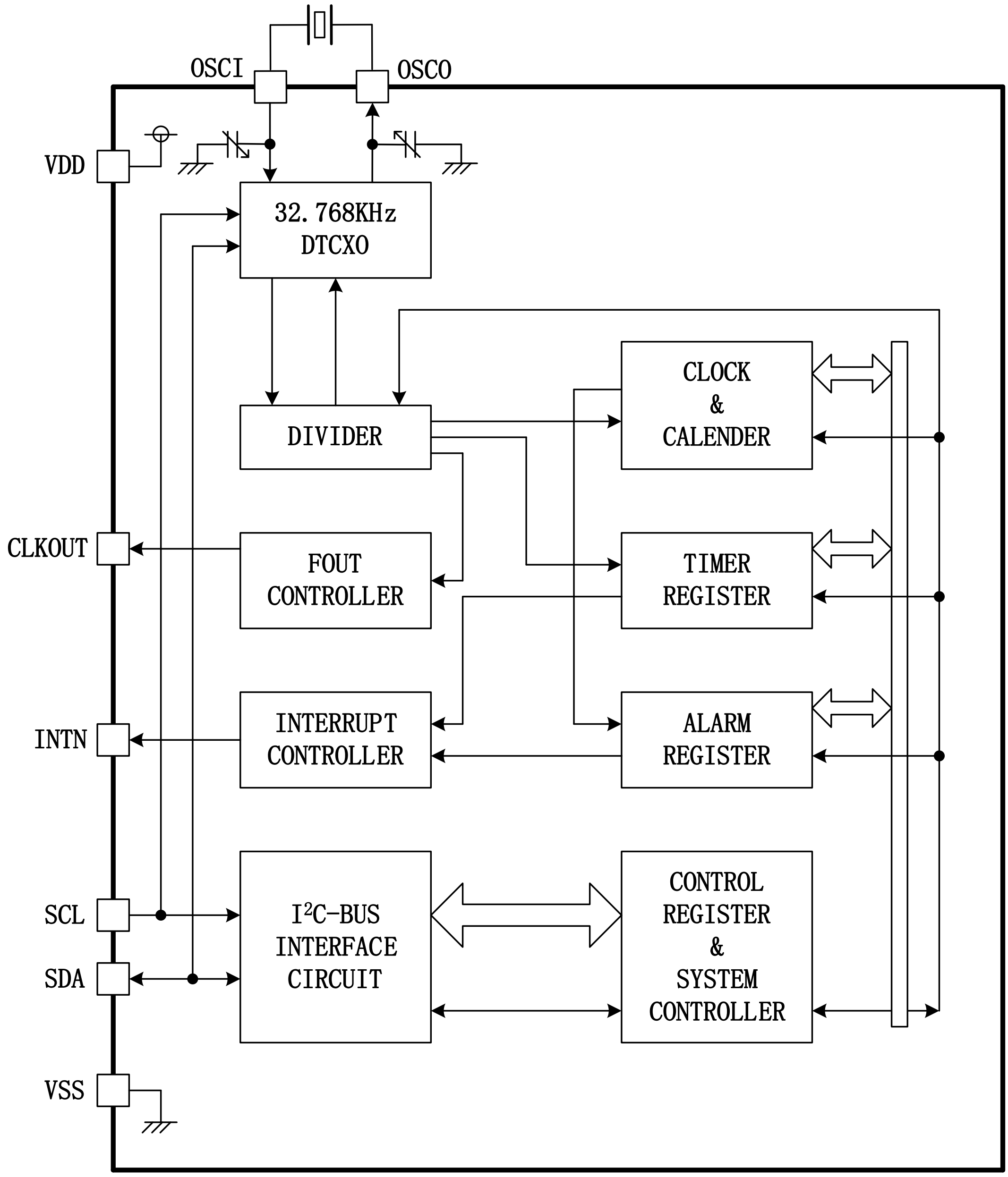


Figure 3-1 JXR260-GA system block diagram

4 Terminal description

4.1 Terminal connections

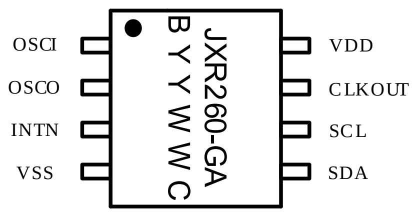


Figure 4-1 JXR260-GA package form

4.2 Pin Description

Table 4-1 JXR260-GA Pin Description

Pin name	I/O	Function
OSCI	IN	oscillator input
OSCO	OUT	oscillator output
INTN	OUT	interrupt output (open-drain; active LOW)
VSS	GROUND	ground
SDA	INOUT	serial data input and output
SCL	IN	serial clock input
CLKOUT	OUT	clock output, open-drain
VDD	POWER	supply voltage

5 Absolute Maximum ratings

Table 4-1 Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply voltag*1	V_{DD}	Voltage between VDD and VSS	-0.5 to 6.5	V
Input voltage*7, *2	V_{IN}	FOE, SCL, SDA pins	-0.5 to V_{DD}+0.3	V
Output voltage*1, *2	V_{OUT}	FOUT, SDA, INTN pins	-0.5 to V_{DD}+0.3	V
Storage temperature	T_{STG}	Store separately, unpacked	-65to 150	ºC

*1: Each electrical indicator shall not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of relevant parameters, reliability reduction and even chip failure.

*2:This V_{DD} refers to the range of V_{DD} under recommended operating conditions.

6 Recommended operating conditions

Table 6-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Interface voltage	2.0	3.0	5.5	V
Clock supply voltage	V_{CLK}	operating voltage of Oscillator module	1.8	3.0	5.5	V
Operating temperaturec range	T_{OPR}	---	-40	25	85	ºC

* Any operation beyond the recommended range in the above table can greatly affect the reliability of the chip.

7 Frequency characteristics

Table 7-1 Frequency Characteristics

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Built-in capacitor	C_{OSC}	Set relative registers	8	25	31	pF
Frequency/voltage characteristics	Δ f/f/V	Ta=25℃		±1.0		$\times 10^{-6}$/V
Oscillator ESR	R_{ESR}	---			150	kΩ
Load Capacitance	C_L	Set relative registers	7		12.5	pF
duty cycle on pin CLKOUT	δ_{CLKOUT}	---		50		%

8 Electrical characteristics

8.1 DC Characteristics

Table 8-1 DC Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{DD1}	f_{SCL} = 400 kHz				800	μ A
	I_{DD2}	f_{SCL} = 100 kHz				200	
	I_{DD3}	interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; Ta=25℃	V_{DD} = 5.0 V		800	1200	nA
	I_{DD4}		V_{DD} = 3.0 V		700	1000	
High-level input voltage	V_{IH}	SCL, SDA pins		0.7*V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}			-0.5		0.3*V_{DD}	V
Low-level output voltage	V_{OL}	CLKOUT, INTN,SDA pins	I_{OL}=1mA	0		0.4	V
Low-level output current	I_{OL}	output sink current; V_{OL} = 0.4 V; V_{DD}=5V	SDA	3			mA
			INTN	1			
			CLKOUT	1			
input leakage current	I_{LK}	SCL, SDA,V_{IN} = V_{DD} or GND		-1		1	μ A
output leakage current	I_{OZ}	CLKOUT, INTN,SDA,V_{IN} = V_{DD} or GND		-1		1	μ A

8.2 AC Characteristics

Table 8-2 AC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	---			400	KHz
Start condition setup time	$t_{SU;STA}$	---	0.6			μS
Start condition hold time	$t_{HD;STA}$	---	0.6			μS
Data setup time	$t_{SU;DAT}$	---	100			nS
Data hold time	$t_{HD;DAT}$	---	0		700	nS
Stop condition setup time	$t_{SU;STO}$	---	0.6			μS
Bus idle time	t_{BUF}	Between start condition and stop condition	1.3			μS
Time when SCL = "L"	t_{LOW}	---	1.3			μS
Time when SCL = "H"	t_{HIGH}	---	0.6			μS
Rise time for SCL and SDA	t_r	---			0.3	μS
Fall time for SCL and SDA	t_f	---			0.3	μS
Allowable spike time on bus	t_{SP}	---			50	nS

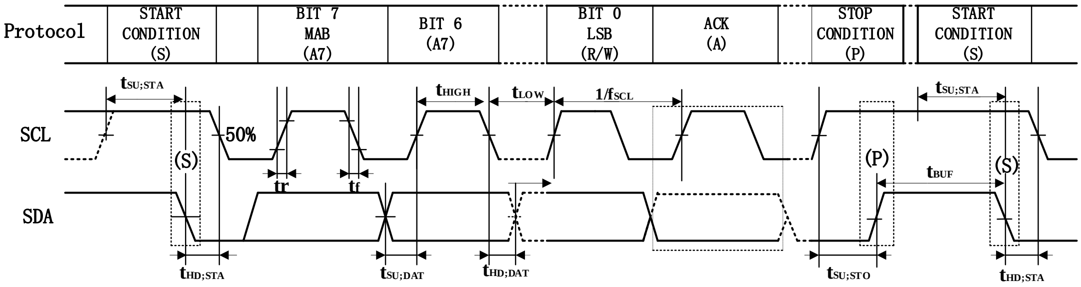


Figure 8-1 IIC timing legend

* The IIC data transfer is located between the start condition and the end condition, and the data transfer operation must be completed within 0.95S time, after which the IIC bus will be reset by the internal timer.

9 Registers

9.1 Register summary table

Table 8-1 Register Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	Control Register 1	TEST1	○	STOP	○	TESTC	○	○	○
01	Control Register 2	○	○	○	TI_TP	AF	TF	AIE	TIE
02	SEC	VDET	40	20	10	8	4	2	1
03	MIN	○	40	20	10	8	4	2	1
04	HOUR	○	○	20	10	8	4	2	1
05	DAY	○	○	20	10	8	4	2	1
06	WEEK	○	○	○	○	○	4	2	1
07	MONTH	○	○	○	10	8	4	2	1
08	YEAR	80	40	20	10	8	4	2	1
09	MIN Alarm	AE_M	40	20	10	8	4	2	1
0A	HOUR Alarm	AE_H	○	20	10	8	4	2	1
0B	DAY Alarm	AE_D	○	20	10	8	4	2	1
0C	WEEK Alarm	AE_W	○	○	○	○	4	2	1
0D	CLKOUT Control	FE	○	○	○	○	○	FD[1]	FD[0]
0E	Timer Counter	TE	○	○	○	○	○	TD[1]	TD[0]
0F	Timer	128	64	32	16	8	4	2	1
10	XOSC Trim	○	○	CL[5]	CL[4]	CL[3]	CL[2]	CL[1]	CL[0]
11	CL Select	○	○	○	○	○	○	CLOP[1]	CLOP[0]
12	Current Adjust	○	○	○	○	○	ADJ[2]	ADJ[1]	ADJ[0]
13	Reserved	○	○	○	○	○	○	○	○
14	Detector Control	○	○	○	○	○	○	○	DETEN

* Make sure to write a legal value to the calendar clock register, otherwise the chip will not be able to perform the correct timing operation.

* Register bits marked with ○ are read-only bits and read values are "0";

*TF, AF bits are only allowed to be written to "0".

*When the chip is powered on, the TESTC，VDET，AE_M，AE_H，AE_D，AE_W，FE，TD[1:0]，DETEN bits are preset to "1", TEST1，STOP，TI_TP，AF，TF，AIE，TIE，FD[1:0]，I20N bits are preset to "0".

9.2 Details of Registers

9.2.1 Control register (registers 00~01)

- **TEST1 bits**

This bit must be set to logic 0 (Default) during normal operations. By setting bit TEST1 in register Control_status_1 the test mode is entered. In such a mode it is possible to set up test conditions and control the operation of the RTC.

In test mode, pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second. The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 26 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0 (STOP must be cleared before the prescaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a one-second increment.

1. Set EXT_CLK test mode (Control_status_1, bit TEST1 = 1).

2. Set STOP (Control_status_1, bit STOP = 1).

3. Clear STOP (Control_status_1, bit STOP = 0).

4. Set time registers to desired value.

5. Apply 32 clock pulses to CLKOUT.

6. Read time registers to see the first change.

7. Apply 64 clock pulses to CLKOUT.

8. Read time registers to see the second change.

- **STOP**

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F2 to F14) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released .

The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz, and 1 Hz.

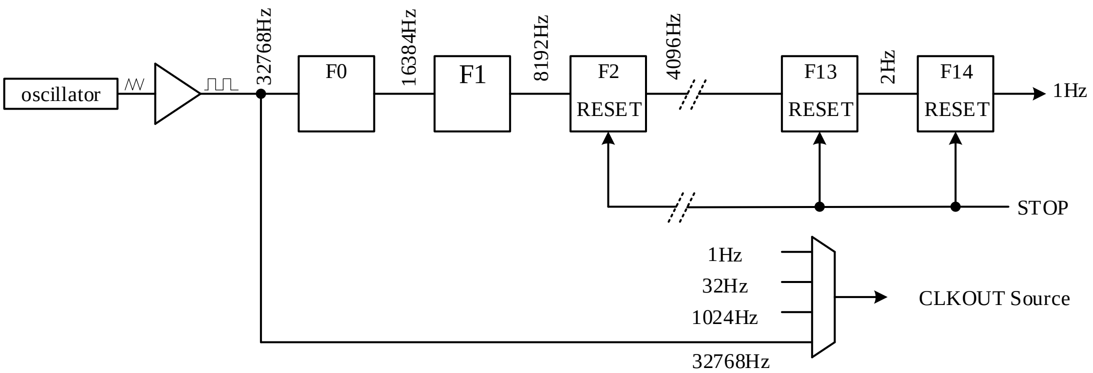


Figure 8-1 STOP bit Function

- **TESTC**

When this bit is ‘0’, Power-On Reset (POR) override facility is disabled; set to logic 0 for normal operation.Power-On Reset (POR) override may be enabled

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I2C-bus pins, SDA and SCL, are toggled in a specific order . All timings are required minimums. Once the override mode has been entered, the device immediately stops, being reset, and normal operation may commence i.e. entry into the EXT_CLK test mode via I2C-bus access. The override mode may be cleared by writing logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.

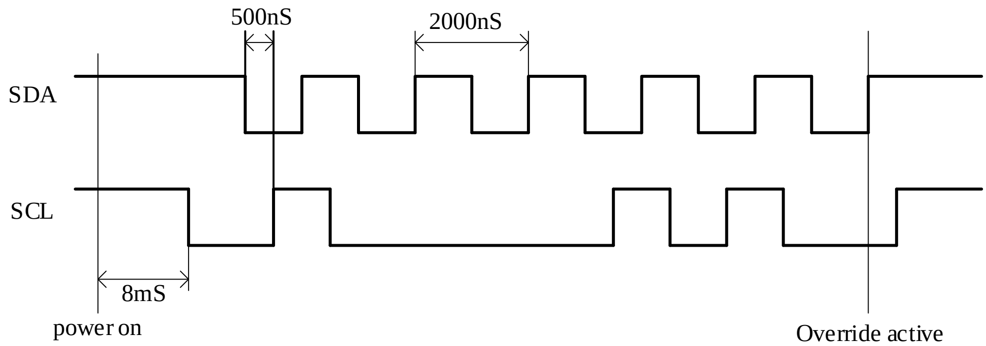


Figure 8-2 POR setting Timing

- **TI_TP**

When a Fixed-cycle timer interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low).

- **AF&TF**

When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten using the interface. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

- **AIE&TIE**

These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

9.2.2 **Time and date registers（Reg 02~08）**

- **VDET**

When the oscillator is stoped, this register will be set to ‘1’. It need to be reset the time. User can set to ‘0’ by IIC.

- **Data form**

With the exception of the week register (register 03 or 13), the data is in BCD code form. For example, the value "0101 1001" in the second register means that it is currently 59 seconds.

The timing mode is fixed to the 24-hour system.

- **Year register and leap year**

The year register ranges from 00 to 99, and then returns to 00 after 99; The year is a leap year when the value represented by the register is divisible by 4. The calendar is valid from 2000 to 2099.

- **Week Register**

The week register has a total of 7 significant bits (bit0~bit2），showed on table 10-2。

Table 8-1 Week registers table

Bit2	Bit1	Bit0	WEEK
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wenessday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

9.2.3 Alarm register（Reg 09~0C）

The alarm can be set to X hours X minutes on X days of the week or X hours X minutes on X days of the month (week alarm mode and day alarm mode), Each Alarm register has AE (Alarm Enable) bits (bit7). When the AE bit of an alarm register is "0", the set value of the register needs to be compared with the corresponding timer register. When the value is consistent, the output alarm is interrupted; If the AE bit is "1", the corresponding alarm register value is ignored, that is, there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is consistent with the corresponding timing register value.

Table 8-2 alarm register bit description

AE_W/D/H/M	WEEK	DAY	HOUR	MIN	Alarm Event
1111	---	---	---	---	Never *Default
1110				Check MINa	Every hour MINa 0 sesond alarm
1101			Check HOURb		Every day HOURb:00:00 alarm
1100			Check HOURb	Check MINa	Every day HOURb:MINa:00 alarm
1011		Check DAYc			Every month DAYcday 00:00:00 alarm
1010		Check DAYc		check MINa	Every month DAYcday 00:MINa:00 alarm
1001		Check DAYc	Check HOURb		Every month DAYc day HOURb:00:00 alarm
1000		Check DAYc	Check HOURb	check MINa	Every month DAYc day HOURb:MINa:00 alarm
0111	Check WEEKd				Every week WEEKd 00:00:00 alarm
0110	Check WEEKd			check MINa	Every week WEEKd 00:MINa:00 alarm
0101	Check WEEKd		Check HOURb		Every week WEEKd HOURb:00:00 alarm
0100	Check WEEKd		Check HOURb	check MINa	Every week WEEKd HOURb:MINa:00 alarm
0011	Check WEEKd	Check DAYc			every week WEEKd & every month DAYcday 00:00:00 alarm
0010	Check WEEKd	Check DAYc		check MINa	every week WEEKd & every month DAYcday 00:MINa:00 alarm
0001	Check WEEKd	Check DAYc	Check HOURb		every week WEEKd & every monthDAYcday HOURb:00:00alarm
0000	Check WEEKd	Check DAYc	Check HOURb	check MINa	every week WEEKd & every month DAYc day HOURb:MINa:00 alarm

9.2.4 CLKOUT Control Register（Reg 0D）

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

- FE

Set FE bit to ‘0’ can disable CLKOUT function, the CLKOUT pin will keep Hi-Z state until set ‘1’ to FE through IIC.

- FD[1:0]

Control CLKOUT frequency, see table10-4.

Table 8-3 CLKOUT Frequency Control

FD[1]	FD[0]	Frequency output @pin CLKOUT
0	0	32.768kHz *Default
0	1	1.024kHz
1	0	32Hz
1	1	1Hz

9.2.5 Timer Interupt Control Regisiter（Reg 0E~0F）

The 8-bit countdown timer at address 0Fh is controlled by the Timer_control register at address 0Eh. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by using the IIC interface.

- **TE**

to enables or disables the timer, ‘0’ disable; ‘1’ enable.

- **TD[1:0]**

determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or 1⁄60 Hz)

Table 9-4 Source Clock Frequency For Timer

TD[1]	TD[0]	Timer Source Clock Frequency
0	0	4.096kHz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz *Default

9.2.6 **Frequency Accuracy Adjust Regisister（Reg 10）**

Output frequency can adjusted by regisister 10h to realize more timer accuracy.

- **CL[5:0]**

The frequency adjust step can refer to table 8-6.

Table 8-5 Frequency adjust step

CL[5:0]	Frequency offset（unit：ppm）		
	CLOP=2’b11(12.5pF)	CLOP=2’b10(9pF)	CLOP=2’b00(7pF)
0	28.8	51.2	108.8
1	27.9	49.6	105.4
2	27.0	48.0	102.0
……	……	……	……
30	1.8	3.2	6.8
31	0.9	1.6	3.4
32 *Default	0.0	0.0	0.0
33	-0.9	-1.6	-3.4
34	-1.8	-3.2	-6.8
……	……	……	……
61	-26.1	-46.4	-98.6
62	-27.0	-48.0	-102.0
63	-27.9	-49.6	-105.4

9.2.7 **Crystal Adaptability Control Regisister（Reg 11）**

JXR260-GA can adapte most of tuning fork crystal oscillator(CL = 7pF, 9pF, 10pF or 12.5pF).

- **CLOP[1:0]**

Table 8-6 configuration to adapte different Crystal

CLOP[1]	CLOP[0]	Load capacitance
0	0	7pF
0	1	10pf
1	0	9pF
1	1	12.5pF *Default

9.2.8 **Current Consumption Adjust Function Regisister（Reg 12）**

JXR260-GA can adjust current consumption by setting regisister 12. The chip can drive the crystal oscillator which ESR is 150kΩ (default). If the ESR of crystal oscillator is less than 150kΩ, user can set regisister 12 for reducing the current consumprion.

- **ADJ[2:0]**

Table 8-7 Current Consumption Adjust

ADJ[2]	ADJ[1]	ADJ[0]	Consumption(nA)
0	0	0	700 *Default
0	0	1	650
0	1	0	600
0	1	1	550
1	0	0	900
1	0	1	850
1	1	0	800
1	1	1	750

9.2.9 **Oscillator State Test Function Regisister（Reg 14）**

Once oscillator is stop, VDET will be set to "1" automatically. If forbid this function, current consumption will reduce 50nA.

- **DETEN**

When DETEN is set to ‘1’(Default), oscillator state test function is on. When DETEN is set to ‘0’, oscillator state test function is off.

10 Interrupt function

10.1 Alarm interrupt

Alarm interrupts can generate an interrupt event for a set week, day, hour, or minute.

10.2 Alarm InterruptTiming

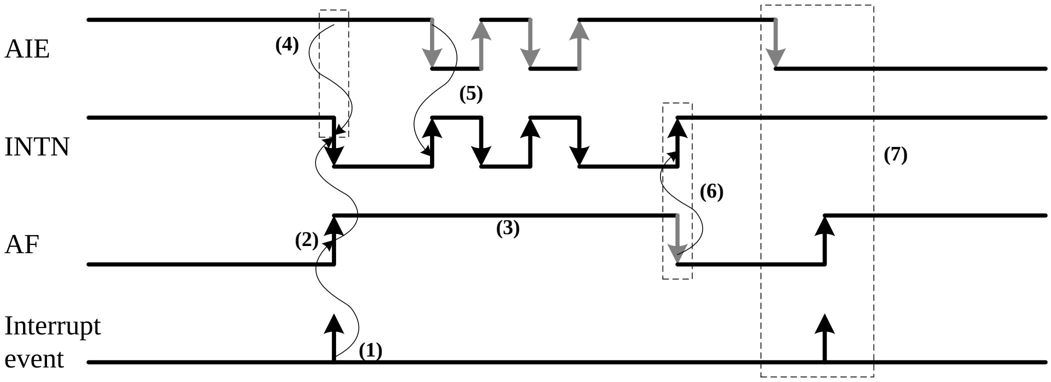


Figure 9-1 Alarm interrupt sequence

(1)Set the hour, minute, date, or week corresponding to the alarm interruption. When the set time matches the current time (for details about the mapping, see Table 10-3), an interruption event is generated

(2)When the alarm interrupt event occurs, the AF flag bit is set to "1".

(3)The AF register will remain "1" until it is manually cleared to "0" via the IIC port.

(4)When the alarm interrupt event occurs, if AIE= "1", INTN outputs a low level; If AIE= "0", INTN remains Hi-Z

(5)If AIE is set to "0" during INTN= "0", INTN immediately returns to the Hi-Z state. AIE can be used to control the output state of INTN before the alarm interrupt event occurs and the AF register is cleared to "0"

(6)Clearing AF register "0" clears the alarm interrupt output, and INTN changes from "0" to Hi-Z status immediately

(7)If AIE= "0" when the alarm interrupt event occurs, INTN remains Hi-Z and does not output low, but the AF flag bit is set to "1".

10.2.1 Alarm interrupt related register

Table 9-1 Alarm interrupt correlation register

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	Control Register 2	○	○	○	TI_TP	**AF**	TF	**AIE**	TIE
09	MIN Alarm	**AE_M**	40	20	10	8	4	2	1
0A	HOUR Alarm	**AE_H**	●	20	10	8	4	2	1
0B	DAY Alarm	**AE_D**	●	20	10	8	4	2	1
0C	WEEK Alarm	**AE_W**	●	●	●	●	4	2	1

- When configuring the alarm interrupt register, it is recommended to set AIE to "0" first to prevent unnecessary hardware interrupts during operation
- The occurrence of the alarm interrupt event will set the AF flag position "1", which will remain "1" until manually set to "0" via the IIC port.
- When the alarm interrupt event occurs, AIE determines whether to generate an interrupt signal output (AIE= "1", then INTN= "0"; AIE= "0", then INTN=Hi-Z)
- An AE_X bit of "0" means that the alarm register needs to be compared with the corresponding clock register; If the AE_X bit is "1", it is not compared with its corresponding clock register, that is, it is considered that the register always matches the corresponding clock register. For details about the mapping relationship, see Table 10-3

10.3 Timed Interrupt

Fixed period interrupts can generate interrupt events at a set period between 244.14 μs and 255min.

10.3.1 Timed Interrupt Timing

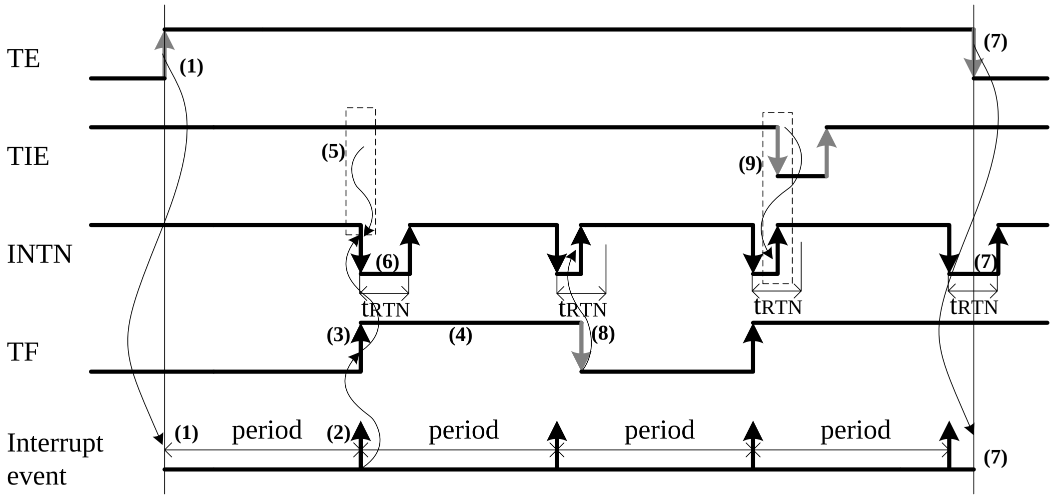


Figure 9-2 Timing interrupt sequence (TI_TP=1)

(1)When the TE bit is written to "1", the fixed period counter counts backwards from the preset value

(2)When the timer counter counts from 01h to 00h, an interrupt event is generated; Counter 0F resets to the preset value and continues the next backward count

(3)TF register is set to "1" when timed interrupt event occurs

(4)The TF register will remain in the "1" state until it is manually cleared to "0" via the IIC port

(5)When the timing interrupt event occurs, if TIE= "1", INTN outputs a low level; If TIE= "0", INTN remains Hi-Z

(6)INTN outputs the low level for t_{RTN}, and then automatically restores the Hi-Z state until the next interruption signal output,$_{RTN}$ as shown in Table 11-3

(7)When TE bit writes "0", timing counter stops counting and INTN outputs Hi-Z (If TE write "0" occurs during INTN= "0", after t_{RTN} time, INTN restores Hi-Z state)

(8)If TF is cleared "0" during INTN= "0", INTN immediately returns to the Hi-Z state

(9)When TIE is written to "0", INTN immediately returns to Hi-Z

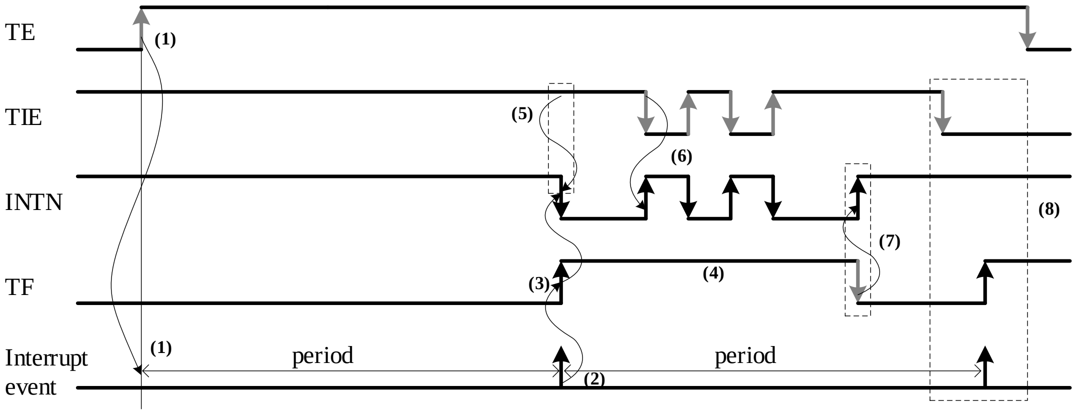


Figure 9-3 Timing interrupt sequence (TI_TP=0)

(1)When the TE bit is written to "1", the fixed period counter counts backwards from the preset value

(2)When the timer counter counts from 01h to 00h, an interrupt event is generated; Counter 0F resets to the preset value and continues the next backward count

(3)TF flag bit is set to "1" when timed interrupt event occurs

(4)The TF register will remain "1" until it is manually cleared to "0" via the IIC port.

(5)INTN outputs a low level if TIE= "1" when a timed interrupt event occurs; If TIE= "0", INTN remains Hi-Z

(6)If TIE is set to "0" during INTN= "0", INTN immediately returns to the Hi-Z state. TIE can be used to controlthe output state of INTN before a timed interrupt event occurs and the TF register is cleared to "0"

(7)Clearing the TF register to "0" clears the timed interrupt output, and INTN changes from "0" to the Hi-Z state immediately

(8)If TIE= "0" when a timed interrupt event occurs, INTN remains Hi-Z and does not output a low level, but the TF flag bit is set to "1".

10.3.2 Timed interrupt correlation register

Table 9-2 Timing interrupt correlation registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	Control Register 2	○	○	○	**TI_TP**	AF	**TF**	AIE	**TIE**
0E	Timer Counter	**TE**	●	●	●	●	●	**TD[1]**	**TD[0]**
0F	Timer	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**

• When configuring the timed interrupt register, it is recommended to set TE and TIE to "0" first to prevent unnecessary hardware interrupts during operation

• TD[1] and TD[0] are used to set the timer clock frequency. The interrupt signal on the INTN pin automatically resets the time t_{RTN} related to the timer clock frequency

• TI_TP is used to control the output form of INTN after the timing interrupt is generated. When TI_TP is set to "0" (Default), TF and TIE are "1", INTN continues to output the interrupt alarm signal; When TI_TP is set to "1", INTN outputs interrupt alarm signal in the form of pulse. For specific low pulse width, refer to Table 11-3

Table 9-3 Timing interrupt count period and automatic reset time

TD[1]	T[0]	Source clock Frequency	Auto reset time	
			n=1	n>1
0	0	4.096kHz	1/8192	1/4096
0	1	64Hz	1/128	1/64
1	0	1Hz	1/64	1/64
1	1	1/60Hz	1/64	1/64

• Register 0F sets the default value of the counter (01h~FFh), and generates a timed interrupt event when the counter counts backwards to 00h in the counting period set by TD[1:0]

• TE is the enable control bit of the fixed period counter. When TE= "1", the counter starts to count backwards; When TE= "0", the counter stops counting and terminates the timing interrupt function

• The occurrence of a timed interrupt event will mark TF position "1", which will remain as "1" until it is manually cleared "0" via the IIC port.

• When a timed interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE= "1", then INTN= "0"; TIE= "0", then INTN=Hi-Z)

Table 9-4 Example timed interrupt period

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μS	15.625mS	1S	1min
……	……	……	……	……
255	62.256mS	3.984375S	255S	255min

11 IIC bus interface

11.1 IIC bus features

IIC is a two-way communication interface, its signal line SDA and clock line SCL need to be connected to VDD through pull-up resistance; The port connected to the IIC bus must be open-drain structure in order to realize the line and connection of multiple devices.

11.2 Data Transmission

1bit of data can be transferred per SCL clock cycle. When sending data, the data on the SDA line changes during the SCL low; When receiving data, stable and effective data can be obtained from the data line SDA during the high level of SCL.

11.3 Start condition and end condition

SCL and SDA remain high when idle. When SCL is high, the falling edge of SDA serves as the starting condition for IIC communication. During the high level of SCL, the rising edge of SDA is used as the termination condition of IIC communication.

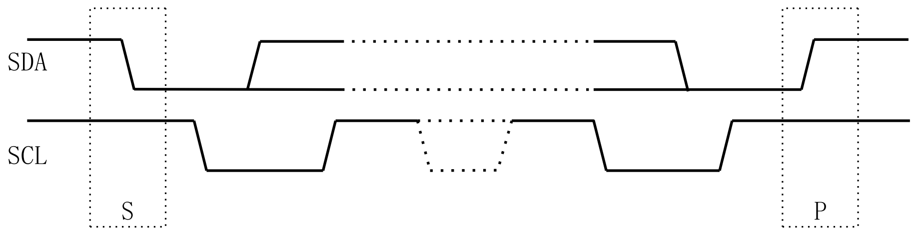


Figure 10-1 IIC start condition and end condition

11.4 Device selection (from address)

The IIC bus device has no chip selection signal, the master device selects the corresponding slave device by sending a unique fixed device number (from the address), and the selected slave device sends a reply signal to establish communication with the master device.

The slave address includes 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2). The slave

address of JXR260-GA is "1010001". During communication, the slave address and R/W select bits are sent as 8bit data.

Slave address							R/W bit
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	0	0	1	R/W

0:write mode
1:read mode

FIG. 10-2 IIC schematic from the address

11.5 System configuration

The device that controls data transmission is called the "master device" and the device controlled by the master device is called the "slave device"; The device that sends the data is called the "sending end" and the device that receives the data is called the "receiving end."

In a JXR260-GA system, the CPU or other control device is the primary device, and the

JXR260-GA chip itself is the secondary device; Both the master and slave devices can be used as sending or receiving ends.

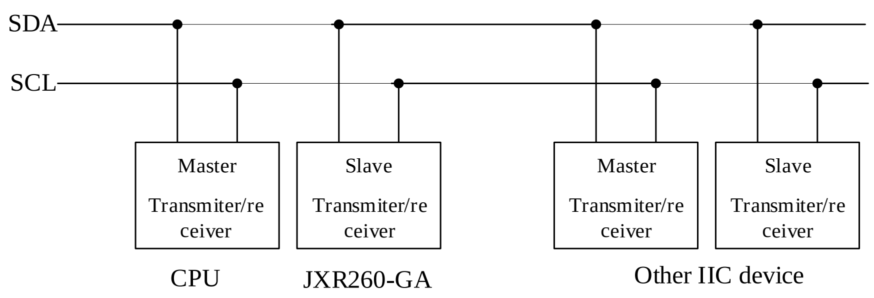


Figure 10-3 IIC system configuration

11.6 Answer signal

The IIC bus has no limit on the number of bytes that can be transferred between the start and end conditions. After each byte of data is transferred, the sender releases the SDA bus and provides an SCL clock to receive the reply signal. If the receiver successfully receives 8 bits of data, the SDA must be set to "0" after the end of the clock for transmitting the last 1bit of data, and the sender will use this low level as the response signal of successful data transmission; After 1 clock cycle, the receiving end releases the SDA bus, ready to receive new data.

The IIC bus terminates the data transfer when the following conditions are met:

(1) When the master device acts as the sender, it sends the termination condition after receiving the reply signal from the slave device.

(2) When the master device acts as the receiver, after successfully receiving 8 bits of data, it sends a "1" as the reply signal and sends the termination condition immediately.

11.7 IIC bus control

This section describes the IIC bus communication timing for the CPU as the master device and the JXR260-GA as the slave device.

11.7.1 Specify address write operations

JXR260-GA has the address automatic increment function, after setting the operation address, only need to send data continuously, the address bit can be automatically incremented.

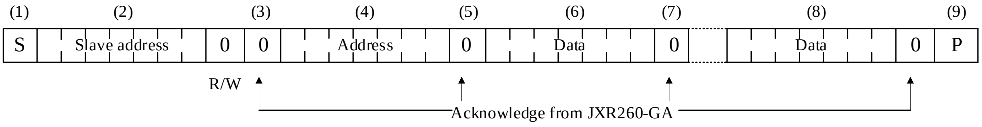


Figure 10-4 Specify the address write operation

(1) CPU send start condition [S]

(2) The CPU sends JXR260-GA from the address and is set to write mode via R/W bit

(3) The JXR260-GA generates an answer signal

(4) The CPU sends the write register address to JXR260-GA

(5) The JXR260-GA generates an answer signal

(6) The CPU sends data to the register corresponding to the address specified in (4)

(7) The JXR260-GA generates an answer signal

(8)Repeat the process (6) (7) and the address of the write register in JXR260-GA will automatically increment

(9) CPU send termination condition [P]

11.7.2 Specify an address read operation

After writing to the register, the CPU can read the register data by setting the read mode.

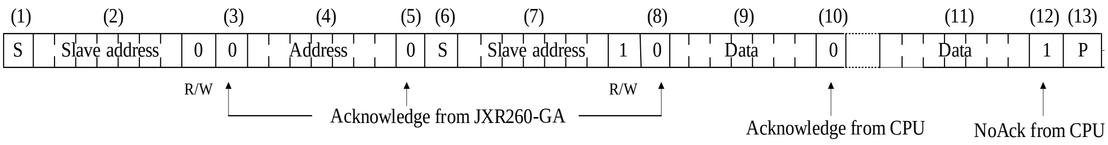


Figure 10-5 specifies the address read operation

(1) CPU send start condition [S]

(2) The CPU sends JXR260-GA from the address and is set to write mode via R/W bit

(3) The JXR260-GA generates an answer signal

(4) The CPU sends the read register address to the JXR260-GA

(5) The JXR260-GA generates an answer signal

(6) The CPU resends the start condition

(7) The CPU sends JXR260-GA from the address and is set to read mode via R/W bits

(8) JXR260-GA generates a response signal; After that, the CPU acts as the receiver and the JXR260-GA acts as the transmitter

(9) The JXR260-GA sends the data in the register corresponding to the address specified in (4)

(10) The CPU sends a reply signal to the JXR260-GA

(11) Repeat the process (9) (10) and the address of the read register in JXR260-GA will automatically increment

(12) The CPU does not send a reply signal to JXR260-GA; The JXR260-GA switches to the IIC data receiver

(13) CPU send termination condition [P]

11.7.3 **Address read operation not specified**

The master device goes directly into read mode to read the contents of all registers from the device. The read operation address is the last IIC operation address +1.

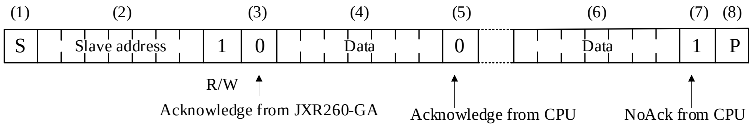


Figure 10-6 does not specify the address read operation

(1) CPU send start condition [S]

(2) The CPU sends the JXR260-GA slave address and is set to read mode via R/W bit

(3) The JXR260-GA generates an answer signal; After that, the CPU acts as the receiver and the JXR260-GA acts as the transmitter

(4) The JXR260-GA automatically increments the register address and sends the register data

(5) The CPU sends a reply signal to the JXR260-GA

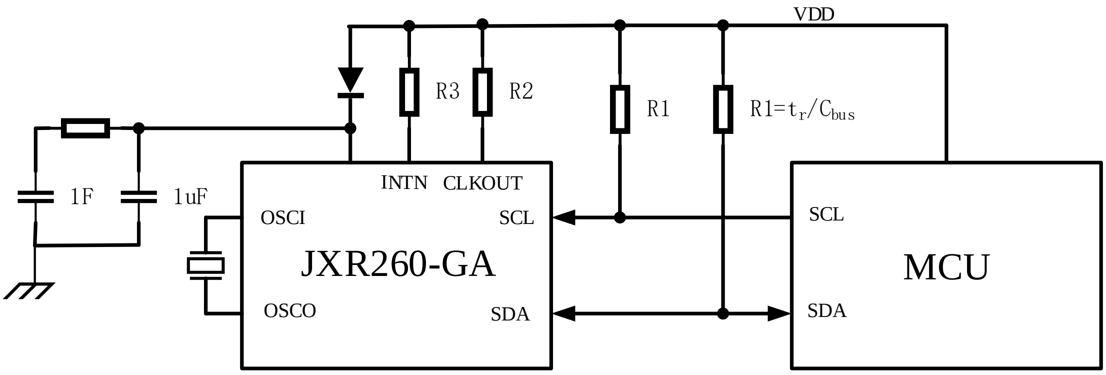
(6)Repeat the process (4) (5) and the address of the read register in JXR260-GA will automatically increment

(7) The CPU does not send a reply signal to the JXR260-GA; The JXR260-GA switches to the IIC data receiver

(8) CPU send termination condition [P]

Addendum

Example Application



• The size of the IIC pull-up resistance should be determined according to the actual communication rate. According to the empirical data, when R1 is 10K Ω , the IIC communication rate of 100KHz can be guaranteed; When R1 is 4.7K Ω , the IIC communication rate of 400KHz can be guaranteed

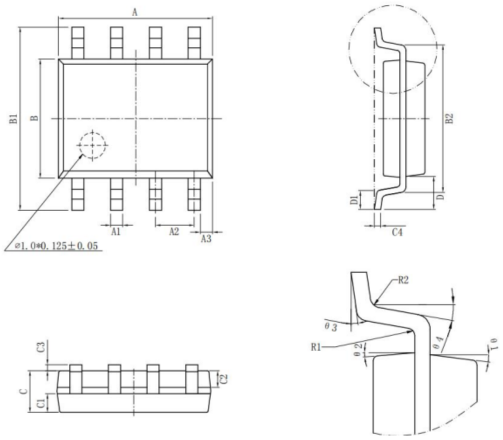
• CLKOUT is an N-Ch open-drain structure, and an external pull-up resistor R2 is needed to measure the frequency output

• In order to avoid unnecessary power fluctuations affecting the chip performance, at least 1uF decoupling capacitor should be added to the chip power pin end (PIN8); The size of the decoupling capacitor varies according to the difference of the user's application environment, so it is necessary to ensure that the chip power supply fluctuation is within the safe range.

• The value of R3 should not be too large to avoid timing errors caused by high level burr of INT output caused by weak pull-up, and the pull-up resistance value is recommended to be about 10K Ω

Package size

SOP8:8pin plastic seal, body 3.9mm wide



DIMENSION	MIN(mm)	MAX(mm)	DIMENSION	MIN(mm)	MAX(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17° TYP4	
C	1.3	1.60	θ2	13° TYP4	
C1	0.55	0.65	θ3	0°~8°	
C2	0.55	0.65	θ4	4°~12°	

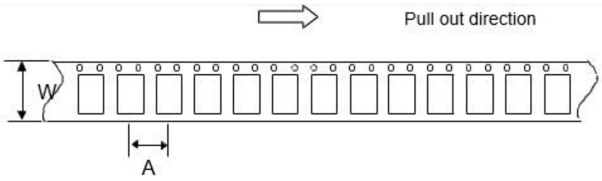
SOP8 package size

SOP8 package specifications

SOP Emboss Taping (TE2)

Symbol	SOP8
A	8
W	12

Unit : mm



Symbol	SOP8
A	330
W	12.4
Contents	4000 pcs

Unit : mm